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A Variation-Tolerant, Stable, Low-Power 6T SRAM Cell in 32-nm CNTFET Technology

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Abstract
The semiconductor industry is focused on the miniaturization of transistors to achieve smaller VLSI circuits. However, downscaling of CMOS technology presents numerous challenges, including unreliability and high leakage. Consequently, carbon nanotube field-effect transistor (CNTFET) has emerged as a promising alternative to traditional CMOS-based transistors, offering superior properties such as improved current handling characteristics and better gate control. Static random-access memory (SRAM) cells are widely used as cache memory in most of electronic devices, but their repetitive structures result in significant power consumption. This paper introduces a robust, low-power, single-ended 6T (SE6T) SRAM cell with high static noise margins. Simulation results conducted using the Stanford University 32-nm CNTFET technology in the HSPICE simulator, with $V_{DD} = 0.4$ V, demonstrate that the proposed SE6T improves RSNM by 1.99 × /3.17 × compared to Conv6T/DCT7T, enhances WSNM by 1.26 × /1.45 × /1.12 × compared to Conv6T/Conv8T/SE8T, and reduces RSNM/WSNM variability by at least 45.24%/41.94%. Regarding power efficiency, the proposed SE6T design shows improvements of 61.82%/50.65%/25.43% in read power compared to Conv6T/DCT7T/SE8T, and reduces write power/leakage power by at least 31.02%/39.33%. Furthermore, the 32-nm CNTFET-based proposed design offers higher robustness, better stability, lower power, and higher speed compared to its 32-nm MOSFET-based counterpart.

Keywords Static random-access memory (SRAM) · Carbon nanotube field-effect transistor (CNTFET) · Read stability · Writability · Low-power consumption

1 Introduction

In the modern era, the widespread adoption of intelligent sensor nodes, portable digital gadgets, and mobile applications has become an integral part of our daily existence. The importance of low-power, stable static random-access memory (SRAM) cells extends

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beyond these applications, encompassing sectors such as transportation, healthcare, agriculture, telecommunications, manufacturing, and the military [28]. Notably, the internet-of-things (IoT) has emerged as a transformative technology that has revolutionized various aspects of industries, offices, homes, and personal lifestyles [27]. Smart homes, smart vehicles, smart agriculture, and smart cities heavily rely on the efficient operation of low-power IoT sensor nodes [27]. The performance of memory devices utilized in these applications hinges on key factors like power efficiency, speed, and stability of SRAM cells. On average, a significant portion of the total power consumption in IoT-based systems is attributed to SRAM memory devices, accounting for approximately 40–50% [32].

A fundamental approach to minimize the aggregate power consumption in SRAM is to decrease the operating voltage. This reduction in voltage has a quadratic impact on dynamic power and a linear influence on leakage power [33]. However, this approach is counterintuitive, as it leads to an increase in delay, subsequently escalating energy consumption. Furthermore, it exacerbates the variability in transistor threshold voltage, thereby compromising transistor performance and circuit reliability [31]. In contrast, the utilization of complementary metal–oxide–semiconductor (CMOS) technology, once a paradigm for achieving dense and power-efficient circuits, is no longer the optimal solution. The increasing complexity of designing such circuits is attributed to the detrimental effects of short-channel behavior, elevated leakage, and parametric variations, among other factors, rendering the designer's task increasingly challenging, if not impossible [4].

Numerous scholarly endeavors have been dedicated to advancing SRAM cells and memory technology in the past. Researchers have introduced a range of techniques, such as multi-threshold transistors, multiple-supply voltage, multiple-voltage logic representation, power-gating, clock-gating, loop-cutting, and decoupled read circuits. These methods aim to create SRAM cells characterized by low-power consumption, robust noise immunity, swift write/read speeds, and the elimination of half-select issues [30]. Instead of focusing solely on circuit-level enhancements to memory systems, the field has seen the adoption of more efficient next-generation field-effect transistors (FETs) like fin-shaped FETs (FinFETs), tunnel FETs (TFETs), graphene nanoribbon FETs (GNRFETs), and carbon nanotube FETs (CNTFETs), which have shown superior performance [12].

The foundational 6T SRAM cell, upon which all existing SRAM cells are based, comprises a storage cell and two access transistors. During the reading process of this cell, the storage nodes directly interact with the bitline, leading to a decrease in its read stability [27]. Hence, to mitigate the issue of reduced read stability, a buffer circuit is employed to decouple the storage nodes from direct communication with the bitline during read operations. This technique is known as the read decoupled technique [32]. An 8T SRAM cell is created by integrating a two-transistor read buffer with a standard 6T SRAM cell, effectively enhancing the read static noise margin (RSNM) of the SRAM cell. However, it's worth noting that the bit line leakage power tends to be higher in the 8T SRAM cell configuration. Incorporating a feedback cutting transistor between the two inverters forming the storage cell of SRAM enhances the write static noise margin (WSNM) by interrupting the feedback loop during write operations. However, it's important to note that this improvement comes at the expense

of increased write delay [30]. In SRAM cells, both single-ended and double-ended methods are utilized for writing and reading bits. These methods employ either pass transistor or transmission gate techniques [12]. Employing stacked transistor-based (PPN or PNN) inverters instead of conventional inverters in SRAM design enhances the hold static noise margin (HSNM) of the bit cell while reducing power consumption and leakage. Additionally, SRAM cells utilizing Schmitt-trigger (ST) based inverters offer low power consumption coupled with high stability. However, in certain SRAM designs, a hybrid bit is formed by combining any two of the following: conventional inverters, ST inverters, and stacked transistor-based inverters. It's important to note that while these hybrid designs offer advantages in terms of power and stability, they may incur increased read delay [11].

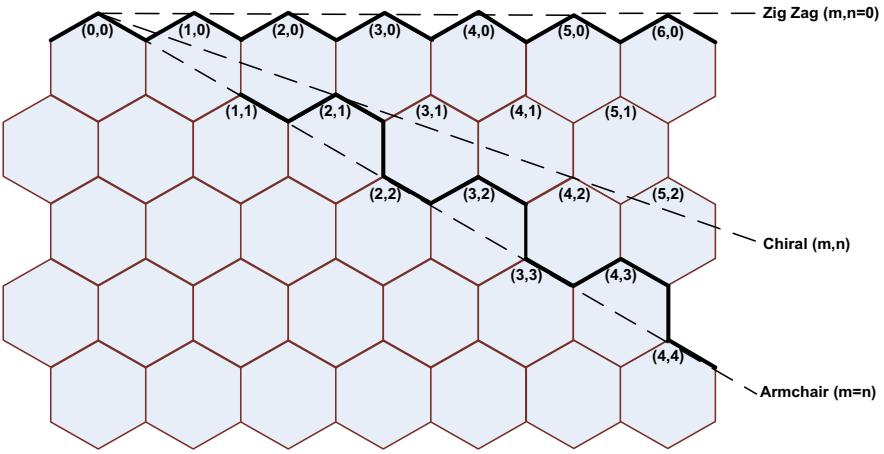
Therefore, this paper presents a novel single-ended six-transistor SRAM cell based on 32-nm CNTFET technology. The main characteristics of the proposed design are as follows:

1. It employs separate reading and writing paths to address transistor sizing issue and to reduce dynamic power consumption.
2. It uses isolated read path to remove read-disturbance issue, thereby, improving read stability.
3. It cuts the GND power rail from one of the inverter to facilitate write operation, thereby, improving writability.
4. It uses minimum-size transistors for the cross-coupled structure to reduce leakage power.

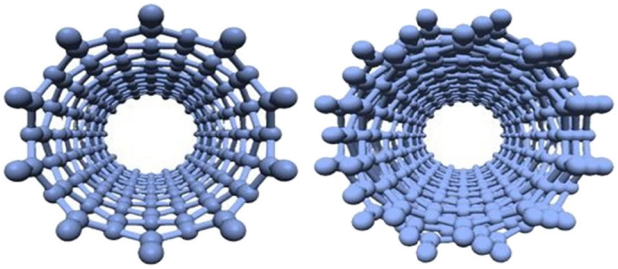
The remaining parts of the paper is structured as follows. Section 2 presents a detailed information about CNTFET devices and related equations. Section 3 reviews the CNTFET-based SRAM cells considered for comparison with this work. The proposed design and its working are presented in Sect. 4. The HSPICE simulation results and discussions are presented in Sect. 5. Section 6 gives a conclusion of this paper.

2 Carbon Nanotube Field-Effect Transistor (CNTFET)

In 1991, Sumio Iijima pioneered the creation of cylindrical fullerenes, known as carbon nanotubes (CNTs). These CNTs exhibit remarkable mechanical, electrical, and thermal properties, making them highly valuable for a wide range of applications, including the biosensors, super-capacitors, energy storage, nano-electromechanical systems, and data storage systems [2, 3, 7]. The electrical characteristics of CNTs are noteworthy. They typically exhibit a current density of approximately 10^9 A/cm and a specific capacity ranging from 39.2 to 90.4 F/cm^3 [36]. The behavior of CNTs can vary significantly based on the choice of chiral vectors (m, n), which are among the most critical parameters. When the chiral vectors satisfy the condition $m = n$ or $|m-n| = 3i$ (where i is an integer), CNTs act as semiconductors. In contrast, if this condition is not met, CNTs function as conductors [23]. Specifically, when n equals m, CNTs are referred to as "armchair," when n is equal to 0, they are termed "zigzag," and when n and m are different, they are categorized as "chiral" [36] (see Fig. 1a).



(a)



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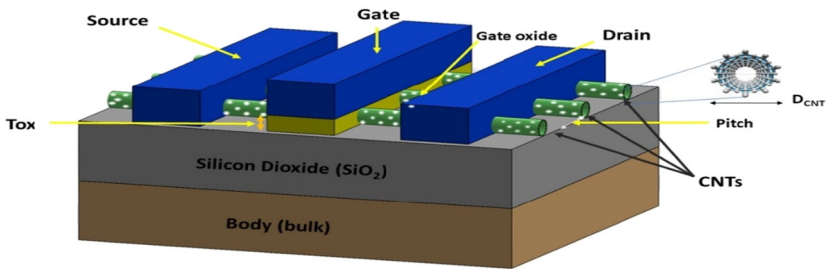


(c)

Fig. 1 **a** Graphene sheet-Honeycomb structure [24], **b** SWCNT (left) and MWCNT (right) structures [6], and **c** cross-sectional schematic of CNTFET [6]

The Eq. (1) shows the relationship between CNT diameter and chirality, where a is the length of the carbon–carbon bond ($a = 2.49$ Å) [36].

$$DCNT = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \tag{1}$$

CNTs are classified into single walled CNT (SWCNT) and multi walled CNT (MWCNT) based on how many tubes are arranged along the axis of the CNT (see Fig. 1b). MWCNT is preferred over SWCNT in most electronics applications due to improper adhesion of SWCNT to the substrate. Also because MWCNT has more number of concentric tubes, active sites are found at its ends. The active sites of MWCNT give better adhesion on the substrate. Besides that the conductivity of MWCNT is higher compared to SWCNT [24].

The structure of the CNTFET (see Fig. 1c) is achieved by using one or more CNTs stacked laterally as the channel instead of the bulk channel in the MOSFET. The distance between the axis of two adjacent CNT-tubes when stacked is called pitch (S). CNTFET technology is available in various configurations, including gate-all-around CNTFETs, ferroelectric junction-less CNTFETs, wrap-gate CNTFETs, pin CNTFETs featuring metal-ferroelectric-metal gating, Negative Capacitance CNTFETs, and Ferroelectric CNTFETs [6].

The channel width of a CNTFET (W_{CNT}), when N number CNTs are utilized is determined by the Eq. (2) [4].

$$W_{CNT} = (N - 1)S + D_{CNT} \tag{2}$$

The gate width (W_g) of CNTFET is given as Eq. (3) [39], where W_{min} is the minimum gate width.

$$W_g = Max(W_{min},\ N\ X\ S) \tag{3}$$

The following equation can be used to calculate a CNTFET's threshold voltage (V_{th}). The equation shows that the V_{th} of CNTFET and that of D_{CNT} are inversely correlated (see Eq. 4) [4].

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \tag{4}$$

where $V_\pi = 3.033$ eV (V_π is energy of the carbon π–π bond) and $e = 1.602 \times 10^{-19}$ (e-electron charge) [4].

3 Existing CNTFET-based SRAM Cells

This section provides an overview of the structures, benefits, and drawbacks of several existing SRAM cells based on CNTFET devices. These cells have been taken into account for comparison with the proposed CNTFET-based SRAM cell in this study.

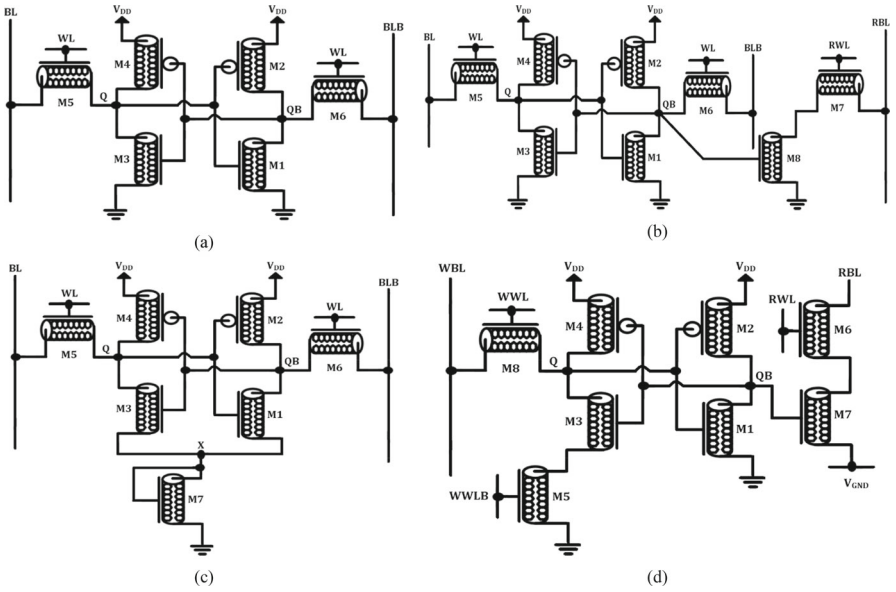


Fig. 2 SRAM cells under investigation **a** Conv6T [23], **b** Conv8T [40], **c** DCT7T [17], and **d** SE8T [30]

3.1 Conventional 6T SRAM Cell

The schematic diagram of the conventional 6T (Conv6T) SRAM cell based on CNTFET devices is depicted in Fig. 2a [23]. It utilizes two conventional inverters M1–M2 and M3–M4 interconnected as cross-coupled to latch the data stored in the internal storing nodes *Q* and *QB*. Two access transistors M5 and M6 are responsible for establishing a pathway to access the cell for executing read or write operations through two bitlines *BL* and *BLB*. In the Conv6T SRAM cell, it is not possible to simultaneously improve RSNM and WSNM because the same access transistors are enabled for both read and write operations. Another drawback of the Conv6T SRAM cell is the issue of half-select disturbance, which causes a writing process to occur in other SRAM cells in the same row of an SRAM array.

3.2 Conventional 8T SRAM Cell

The conventional 8T (Conv8T) SRAM cell, as illustrated in Fig. 2b [40], introduces a single-ended structure consisting of M7 and M8, along with a read wordline (*RWL*) and a read bitline (*RBL*), to the Conv6T SRAM cell. This structure is utilized for performing read operations. When $RWL = $ '1', the V_{DD}-precharged *RBL* is discharged to the ground through M7–M8 or remains unchanged, depending on *Q* node's content. This completely isolates the internal storing nodes *Q* and *QB* from the *RBL*, resulting in a significant improvement in RSNM comparable to HSNM. The single-ended reading structure reduces the power consumption during the read operation by recuing the bitline activity factor and increases the read delay. By incorporating separate paths for

reading and writing, the Conv8T SRAM cell eliminates the need for transistor sizing requirements present in the Conv6T SRAM cell. However, it is important to note that the decoupled read path implemented in the Conv8T SRAM cell is the primary source of leakage, which escalates with the scaling of technology. Additionally, the increased number of bitlines exacerbates the power dissipation caused by leakage.

3.3 Diode-Connected Transistor 7T SRAM Cell

The structure of the diode-connected transistor 7 T (DCT7T) SRAM cell is illustrated in Fig. 2c [17]. This cell combines a Conv6T SRAM cell with an additional diode-connected transistor (M7) placed between the sources of M1-M3 and the ground. The reading and writing operations in the DCT7T SRAM cell are carried out similarly to those in the Conv6T SRAM cell. As a result, it experiences the read-disturbance issue and transistor sizing requirements should be considered into consideration. The presence of M7 results in an increase in the voltage of the X node (V_X) by ΔV compared to the ground potential. This introduces both advantages and disadvantages. On the positive side, this technique helps reduce the overall leakage current since V_X is no longer at ground potential. However, it also leads to an increase in the read delay as the discharging path for the bitlines becomes longer. On the other hand, the inclusion of M7 weakens the pull-down networks of the latch core formed by M1-M4. As a result, it reduces HSNM and RSNM, while increasing WSNM and the writing speed.

3.4 Single-Ended 8T SRAM Cell

The SRAM cell known as single-ended reading/writing 8 T (SE8T), as depicted in Fig. 2d [30], utilizes separate paths for reading and writing operations, thereby, eliminating the need for transistor sizing requirements. It consists of two conventional cross-coupled inverters (M1–M4) and an additional transistor (M5) controlled by the write wordline bar (*WWLB*), positioned between the source of M3 and the ground. The SE8T SRAM cell employs two transistors (M6 and M7), one read bitline (*RBL*), and two control signals (*RWL* and V_{GND}) to construct a single-ended reading structure. During a read operation, *RWL* and V_{GND} are set to '1' and '0', respectively. The V_{DD}-precharged *RBL* is either discharged to the ground through M6–M7–V_{GND} or remains unchanged, depending on the data stored in Q. This resolves the read-disturbance issue and improves the RSNM to a level as high as the HSNM.

The adoption of single-ended structures for both reading and writing operations reduces dynamic power consumption but degrades speed performance. Additionally, the elimination of leakage in the reading path reduces power dissipation due to leakage. In the write '0' process, M8 needs to be stronger enough than M4 to flip the content of Q. The fighting between transistors M4 and M8 results in a negative impact on the WSNM.

4 Proposed CNTFET-Based Single-Ended 6T SRAM Cell

The schematic diagram of the proposed CNTFET-based single-ended reading/writing 6T (SE6T) SRAM cell, along with its timing diagram, is presented in Fig. 3. It utilizes two conventional inverters composed of transistors M1-M2 and M3-M4, which are connected in a back-to-back configuration. The source of transistor M3 is controlled by the V_{GND} signal. This cross-coupled structure of the inverters ensures the retention of data stored in the internal storing nodes Q and QB. Table 1 provides an overview of the status of the various control signals and bitlines used in the proposed SE6T SRAM cell during different operational modes. The following subsections describe the working of the proposed design in hold, read, and write modes of operation.

4.1 Hold Operation

The suggested SE6T SRAM cell is required to potentially retain the contents of the internal storing nodes Q and QB during the hold mode. To supply the source of M3,

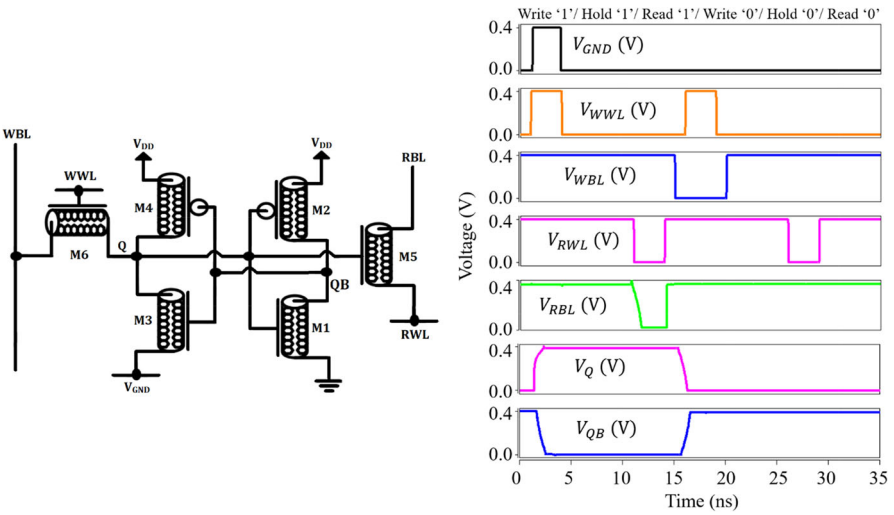


Fig. 3 Proposed CNTFET-based single-ended 6T (SE6T) SRAM cell, along with its timing diagram

Table 1 Status of the signals and bitlines of the proposed SE6T SRAM cell in the different operation modes

Signals/Bitlines	Hold	Read	Write '0'/ '1'
RBL	V_{DD}	V_{DD} (precharged)	V_{DD}
WBL	V_{DD}	V_{DD}	GND/V_{DD}
RWL	GND	V_{DD}	GND
WWL	GND	GND	V_{DD}
V_{GND}	GND	GND	GND/V_{DD}

V_{GND} is set to GND, which enables the pull-down network of the left inverter. To minimize leakage in the reading path, *RBL* and *RWL* are set to V_{DD}. To remove the writing path, *WWL* is set to GND, which turns off M6. As a result, the cross-coupled inverters M1 to M4 effectively preserve the data stored in the cell.

4.2 Read Operation

The proposed SE6T SRAM cell utilizes a single-ended reading structure to execute the read operation through the M5 transistor, *RWL* signal, and *RBL* bitline. Prior to initiating the read operations, *RBL* is precharged to V_{DD}. The read operations are initiated by pulling down the *RWL*. During these operations, *WWL* is set to GND to deactivate M6 and remove the writing path. V_{GND} is set to GND to connect the source of the M3 to the ground, and *WBL* is set to V_{DD}. Depending on the content stored in the internal storing node *Q*, *RBL* is either discharged to the ground through M5-*RWL* or remains unaltered.

Figure 4a depicts the read '0' operation and the sneaking current in the proposed SE6T SRAM cell. The figure comprises three cells, namely Cell 1, Cell 2, and Cell 3, arranged in a column with varying conditions. The columnar *RBL* has been precharged

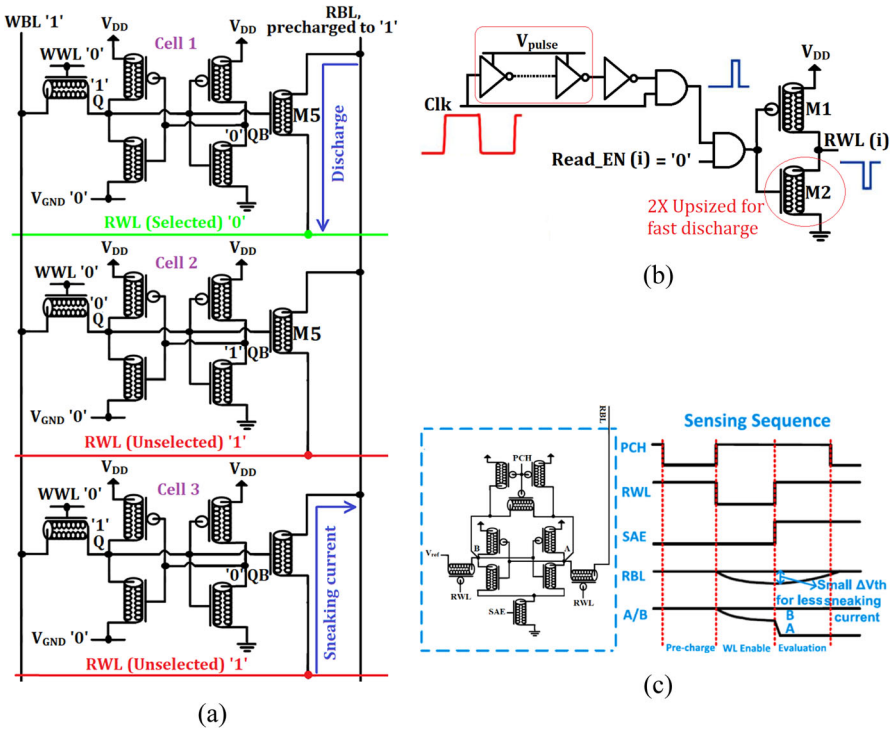


Fig. 4 **a** Read '0' operation and Sneaking current in the proposed SE6T SRAM cell, **b** RWL driver [39], and **c** Differential sense amplifier circuit [21]

to V_{DD} initially. In Cell 1, the row-based *RWL* is pulled down to the ground, indicating that the reading cycle has been initiated. The internal storing nodes *Q* and *QB* have been initially set to '1' and '0', respectively. Consequently, M5 is turned on, providing a path for *RBL* to discharge to the ground through M5-*RWL*.

Cell 2 stores '0'/'1' logic in its internal storing node *Q*/*QB*. In this cell, the *RWL* is in an unselected mode, set to V_{DD}. M5 is in the *OFF*-state, and there is no leakage from *RBL* to *RWL*.

Cell 3 has the same conditions as Cell 1, except that its *RWL* is set to V_{DD}. In this cell, a sneak current path emerges, leading to two problems: (1) increased short circuit power during the read operations and (2) incorrect sensing due to *RBL* discharge slowdown [21, 39]. To address these issues, we have considered two strategies mentioned below. Since *RWL* is enabled for all cells placed in a row, the *RWL* driver must have the ability to sink the current through all turned-on M5 transistors. Additionally, the *RWL* driver must generate a pulsed *RWL* signal so that the selected *RWL* is enabled only for a shorter duration. The *RWL* driver is illustrated in Fig. 4b [39]. In the *RWL* driver, the transistor M2 has been upsized 2X, i.e., having two CNTs, for fast *RBL* discharge. On the other hand, a differential sensing scheme shown in Fig. 4c has been employed [21]. During read operations, the sense amplifier enable (*SAE*) signal is pulled up to the V_{DD} to start the sense amplifier working to sense the *RBL* signal. When the V_{DD}-precharged *RBL* is discharging and falls below the reference voltage (V_{ref}), or less than 10% of its precharged potential, the small difference change in *RBL* voltage will be distinguished. Compared with inverter based sensing, the differential cross-coupled sense amplifier can improve read speed by 30% because of small signal sensing and save power by 25% due to elimination of sneaking current and short-circuit current [21].

4.3 Write Operation

The proposed SE6T SRAM cell utilizes a single-ended writing structure to write the desired logic to the cell. This is achieved through the use of the write-access path M6, *WWL* signal, and *WBL* bitline. During the writing operations, both *RWL* and *RBL* are maintained at a high logic level (V_{DD}). The data to be written to the cell is applied on the *WBL*, and *WWL* is raised to V_{DD} to activate M6 and provide the writing path. Depending on the data applied on *WBL*, V_{GND} is either raised to V_{DD} or kept at GND.

Figure 5a demonstrates the writing process for a logic '1' in the proposed SE6T SRAM cell. The initial logics stored in the *Q* and *QB* are '0' and '1', respectively. A logic '1' is applied on *WBL*, and the write-access transistor M6 is activated by enabling *WWL*. The source of M3 is connected to V_{DD} by setting V_{GND} to V_{DD}, which weakens the pull-down network of the inverter M3–M4. The logic '1' is then easily written to the *Q* node through *WBL*-M6. Additionally, there is an additional charging path for the *Q* node through V_{GND}-M3 at the initial time. When the voltage of the *Q* node reaches the switching voltage of the inverter M1–M2, the *QB* node is flipped, and M4 is activated to charge the *Q* node to V_{DD}.

The writing process for a logic '0' in the proposed SE6T SRAM cell is shown in Fig. 5b. The *WBL* is set to '0', *WWL* is raised to V_{DD}, and V_{GND} is grounded. The

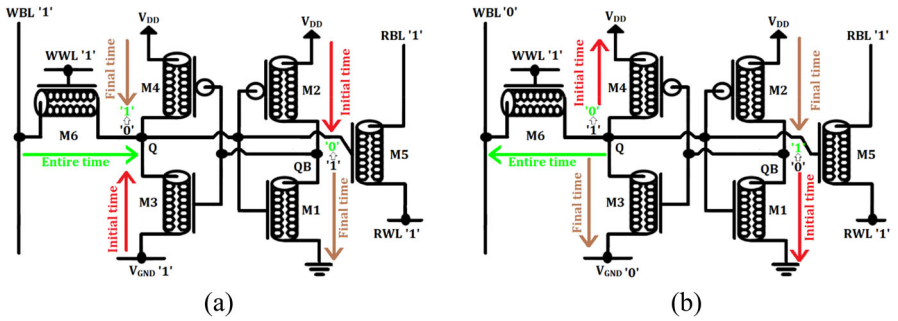


Fig. 5 **a** Write '1' and **b** Write '0' operations in the proposed SE6T SRAM cell

logic '0' is written to the Q node through M6-*WBL*. Right after the inverter M1-M2 is switched, the QB node is charged to V_{DD} through M2. Therefore, M3 is activated and connects the Q node to the grounded-V_{GND}. There is a fighting between M6 and M4 at initial time of writing process, so M6 needs to be stronger than M4 to discharge the Q node to the grounded-*WBL*.

5 Simulation Results and Discussions

5.1 Simulation Setup

The proposed SE6T SRAM cell underwent simulation using the Synopsis HSPICE simulator, employing the compact model for CNTFET [14, 15]. This specific model from Stanford University [35] is designed for enhancement mode unipolar MOSFET-type CNTFETs, where each transistor consists of one or more CNTs serving as its channel. The model takes into consideration various non-idealities, such as Schottky effects, elastic scattering in the channel region, screening effect by the parallel CNTs in CNTFETs with multiple CNTs, and parasitic components including source/drain and gate capacitances and resistances. The main CNTFET parameters, along with their values and descriptions, have been presented in Table 2 [14, 15, 35].

The different performance metrics of the proposed SRAM cell, including RSNM, WSNM, read delay, write delay, read power, write power, and leakage power, have been evaluated and compared with other existing CNTFET-based SRAM cells, namely Conv6T [23], DCT7T [17], Conv8T [40], and SE8T [30], as illustrated in Fig. 2. To ensure a fair comparison, all the investigated SRAM cells have been re-simulated in this study based on the CNTFET parameters tabulated in Table 2. Moreover, to ensure a meaningful comparison and analysis of the simulation results, a 2 Kb SRAM memory (64×32 array) has been designed for all the SRAM cells under investigation in this study.

Since the Conv6T SRAM cell necessitates accurate sizing for successful reading and writing operations, we have assigned three CNTs to its pull-down transistors M1 and M3, two CNTs to its access transistors M5 and M6, and one CNT to its

Table 2 Used CNTFET model parameters [14, 15, 35]

Parameter	Description	Value
L_{ch}	Channel length	32 nm
$L_{S/D}$	Source/Drain length	32 nm
L_{geff}	The mean free path in the intrinsic CNT	100 nm
E_{fo}	Fermi level	0.6 eV
T_{ox}	Oxide thickness	4 nm
K_{ox}	Dielectric material for top gate	16
(m, n)	Tube chiral vector	(19, 0)
V_{th}	Threshold voltage	0.289 V
S	Intertube space of CNT	20 nm
V_{fbn} and V_{fbp}	nCNTFET & and pCNTFET flatband voltage	0.0 V and 0.0 V

Table 3 The number of CNTs used for each transistor in the comparison SRAM cells

SRAM cell	Transistor	No. of CNTs
Conv6T [23]	M1 and M3	3
	M2 and M4	1
	M5 and M6	2
DCT7T [17]	M1, M3, and M7	3
	M2 and M4	1
	M5 and M6	2
Conv8T [40]	M1, M2, M3, M4, M7, and M8	1
	M5 and M6	2
SE8T [30]	M1, M2, M3, M4, M5, M6, and M7	1
	M8	2
SE6T	M1, M2, M3, M4, and M5	1
	M6	2

pull-up transistors M2 and M4. The DCT7T SRAM cell also has the same count of CNTs as the Conv6T cell due to sharing the access paths between reading and writing processes. In the remaining SRAM cells, the cell core contains transistors with one CNT, the read-access transistors have one CNT, and the write-access transistors have two CNTs. Table 3 provides information regarding the number of CNTs assigned to each transistor of the comparison SRAM cells.

5.2 Read Static Noise Margin

An SRAM cell should strive to maintain stability during the read operation. The level of stability is determined by the RSNM, which represents the maximum DC noise voltage that the SRAM cell can tolerate without losing the stored contents in its storing nodes

[26]. The RSNM of the SRAM cell is evaluated by analyzing the voltage transfer characteristic (VTC) or butterfly curve of the back-to-back connected inverters during the read operation and determining the side length of the largest embedded square in the smaller wing of the butterfly curves [5, 40].

The read butterfly curves for the Conv6T and proposed SE6T SRAM cells at different V_{DD} values are illustrated in Fig. 6a and b, respectively. In the Conv6T, the presence of the read-disturbance issue leads to a degradation in RSNM. However, in the proposed SE6T, the internal storing nodes are completely isolated from the read bitline through the use of an isolated reading path, resulting in an improvement in RSNM. As depicted in Fig. 6, the proposed SE6T demonstrates RSNM enhancements of 1.99, 1.97, 2.02, and 2.15 times compared to the Conv6T [23] at V_{DD} values of 0.4, 0.5, 0.6, and 0.7 V, respectively.

Figure 7 presents the read butterfly curves for all the investigated SRAM cells at V_{DD} = 0.4 V. Both the Conv6T and DCT7T SRAM cells experience the read-disturbance issue due to the lack of an isolating reading path, resulting in lower RSNM compared to the other studied SRAM cells. The introduction of the diode-connected transistor

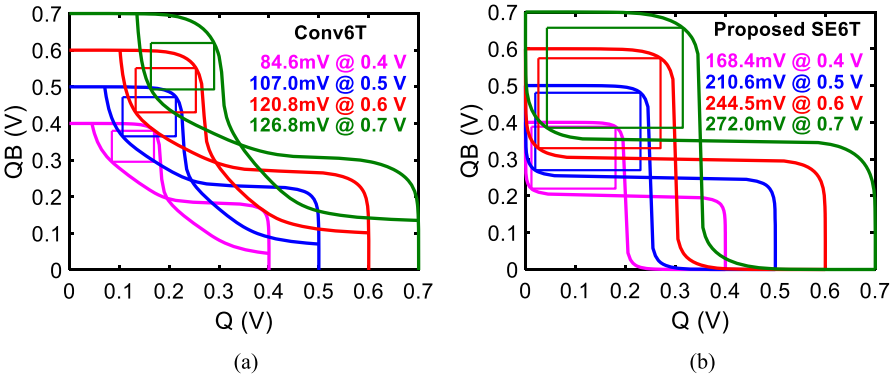
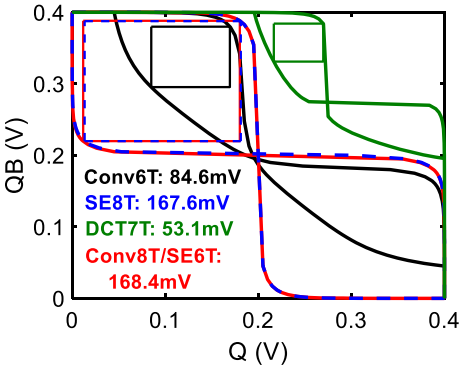


Fig. 6 Read butterfly curves versus V_{DD}, **a** Conv6T and **b** Proposed SE6T

Fig. 7 Read butterfly curves for the investigated SRAM cells at $V_{DD} = 0.4$ V



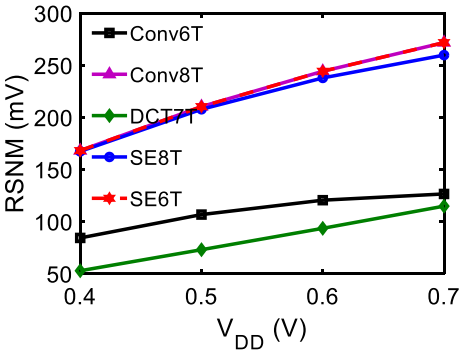


Fig. 8 RSNM for the understudy SRAM cells versus V_{DD}

(M7) increases the voltage V_X, which weakens the pull-down networks of the cross-coupled inverters, thereby further degrading RSNM. The RSNM of the Conv8T, SE8T, and proposed SE6T SRAM cells is improved by utilizing a read-decoupling technique to isolate the storing nodes of the latch core from the read bitline. As shown in Fig. 7, the proposed SE6T design enhances RSNM by 1.99 and 3.17 compared to the Conv6T [23] and DCT7T [17] SRAM cells, respectively, and achieves comparable RSNM to the Conv8T [40] and SE8T [30] SRAM cells at $V_{DD} = 0.4$ V. Additionally, Fig. 8 illustrates the RSNM of the investigated SRAM cells as a function of V_{DD}. The proposed SE6T and Conv8T SRAM cells exhibit the highest RSNM values across all the simulated V_{DD} values.

5.3 Write Static Noise Margin

In the proposed SE6T SRAM cell, which uses a single-ended writing structure, writing a '1' is more challenging than writing a '0'. The WSNM for writing a '1' is estimated and recorded for all the studied SRAM cells. Figure 9a and b illustrate the combined read and write VTCs for the Conv6T and proposed SE6T SRAM cells at different

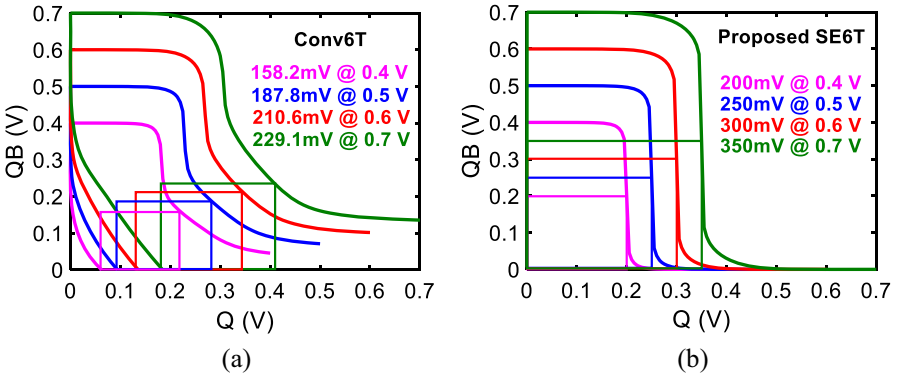


Fig. 9 WSNM versus V_{DD}, **a** Conv6T and **b** Proposed SE6T

V_{DD} values. It is observed that the proposed SE6T design improves WSNM by 1.26, 1.33, 1.42, and 1.53 times compared to the Conv6T [23] at V_{DD} values of 0.4, 0.5, 0.6, and 0.7 V, respectively. These improvements are attributed to the utilization of a write-assist technique, which breaks the pull-down path for the '0' storage node Q and provides an additional charging path through V_{GND}-M3. Figure 10 shows the combined read and write VTCs for all the investigated SRAM cells at $V_{DD} = 0.4$ V. Due to the aforementioned reasons, the proposed SE6T SRAM cell exhibits 1.26, 1.45, and 1.12 times higher WSNM compared to the Conv6T [23], Conv8T [40], and SE8T [30] SRAM cells, respectively. However, it incurs a 1.15 times penalty in WSNM compared to the DCT7T [17]. This is because the application of M7 in the DCT7T acts as a diode-connected transistor, increasing the voltage at node X and weakening the pull-down network. The utilization of a fully differential structure in the DCT7T further enhances WSNM. Figure 11 illustrates the WSNM for all the studied SRAM cells as a function of V_{DD}. The proposed SE6T SRAM cell exhibits the second-highest WSNM among all the studied SRAM cells for all considered V_{DD} values.

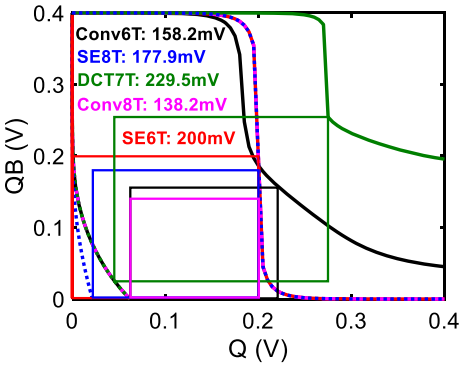


Fig. 10 WSNM for the investigated SRAM cells at $V_{DD} = 0.4$ V

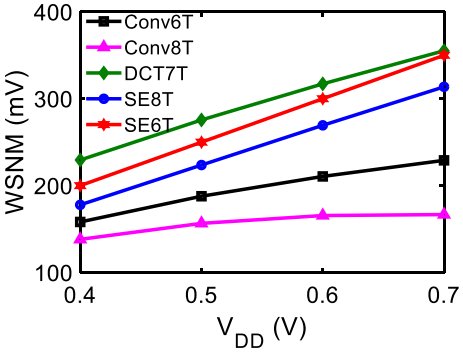


Fig. 11 WSNM for the understudy SRAM cells versus V_{DD}

5.4 Read/Write Access Time

To assess the speed of an SRAM in performing read and write operations, we utilize the concepts of read access time (or read delay) and write access time (or write delay) [8]. These measures can be determined using the following definitions. The read delay is defined as the period between the activation of the wordline responsible for the read operation and the time it takes to discharge the corresponding bitline voltage by 10% [14]. The write delay refers to the time interval between the write wordline activation and the completion of charging (or discharging) the '0'/'1' storing node to 90% (or 10%) of V_{DD} [6]. Since the SE6T design we propose utilizes a single-ended writing scheme and the process of writing '1' is more challenging than that of writing '0', we compare all the SRAMs in terms of their write '1' delay.

Figure 12a presents a comparison of the read delay for the SRAMs under investigation at different V_{DD} values. The Conv6T SRAM exhibits the shortest read delay among the analyzed SRAMs due to its utilization of a differential reading structure and the presence of enlarged transistors that contribute to the reading operations. On the other hand, the DCT7T SRAM, despite employing a differential reading structure and wider transistors, experiences the highest read delay. This is attributed to the implementation of a diode-connected transistor (M7), which elongates the reading path and causes a shift of V_X to a higher potential than the ground potential. These two factors significantly contribute to the increase in read delay. Among the single-ended reading SRAMs (Conv8T, SE8T, and proposed SE6T), the proposed SE6T demonstrates the lowest read delay as it utilizes only one read-access transistor (M5). The Conv8T and SE8T SRAMs exhibit a comparable read delay due to the presence of two series-connected transistors in their reading path. However, the SE8T displays a slightly higher read delay, primarily because of its usage of a row-based V_{GND} signal. At V_{DD} = 0.4 V, the proposed SE6T SRAM achieves significant reductions in read delay compared to other SRAMs. Specifically, it reduces the read delay by 78.41% compared to the DCT7T [17], by 23.53% compared to the Conv8T [40], and by 30.85% compared

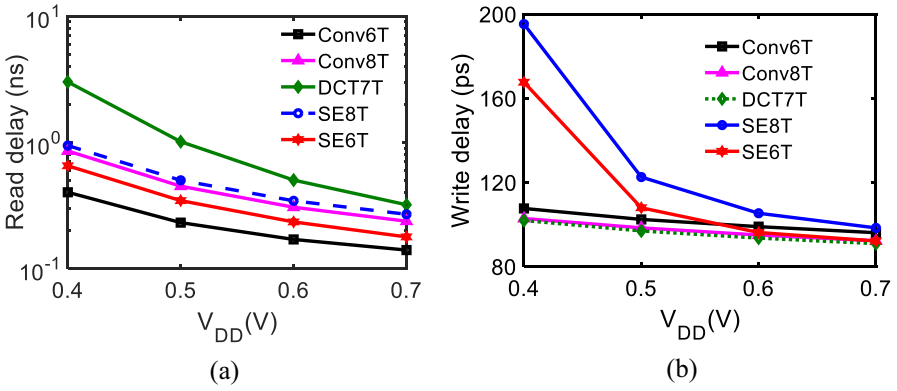


Fig. 12 Delay for the understudy SRAMs versus V_{DD}, **a** Read delay and **b** Write delay

to the SE8T [30]. Nevertheless, it is important to note that the proposed SE6T exhibits a 1.63 times higher read delay compared to the Conv6T [23].

Figure 12b illustrates a comparison of the write delay among the investigated SRAMs at different V_{DD} values. The SRAMs employing a differential writing scheme, namely Conv6T, DCT7T, and Conv8T, exhibit lower write delay compared to SRAMs with a single-ended writing structure, namely SE8T and proposed SE6T. The inclusion of a diode-connected transistor (M7) in the DCT7T weakens the pull-down network of the cross-coupled inverters by shifting V_X to a voltage higher than the ground potential. Consequently, the writing process becomes easier for the DCT7T compared to other analyzed SRAMs. The Conv8T demonstrates shorter write delay compared to the Conv6T due to the utilization of write-access transistors that are wider than the pull-down/up transistors. In both the SE8T and proposed SE6T, the pull-down network corresponding to the '0' storing node Q is weakened to facilitate the writing '1' process. However, the proposed SE6T exhibits lower write delay because it benefits from an additional charging path formed by V_{GND}-M3 for the '0' storing node Q. At $V_{DD} = 0.4$ V, the proposed SE6T reduces the write delay by 16.15% compared to the SE8T [30]. However, it is important to note that the proposed SE6T SRAM experiences 1.56, 1.64, and 1.63 times higher write delay compared to the Conv6T [23], DCT7T [17], and Conv8T [40], respectively.

5.5 Dynamic Power

A significant portion of an SRAM's overall power consumption is derived from dynamic power, primarily resulting from the charging and discharging of capacitances associated with the bitlines [26]. Additionally, the activation of various control signals to execute specific operations contributes to the dynamic power usage [15]. The dynamic power can be mathematically represented by Eq. (8), wherein $\alpha_{bitline}$, C_{Eff}, V_{DD}, and f represent the switching activity factor of the bitline, effective capacitance, power supply voltage, and reading/writing frequency, respectively [6, 39]. Based on Eq. (8), it can be inferred that an SRAM employing a differential structure exhibits higher dynamic power consumption since $\alpha_{bitline}$ equals 1, whereas in an SRAM using a single-ended structure, $\alpha_{bitline}$ decreases to less than 0.5 [35, 40].

$$P_{Dynamic} = \alpha_{bitline} \times C_{Eff} \times V_{DD}^2 \times f \tag{8}$$

Figure 13a presents a comparison of the read power consumption among the investigated SRAMs at different V_{DD} values. The SRAMs utilizing the Conv6T and DCT7T designs exhibit higher read power consumption compared to the other SRAMs. This is primarily due to their implementation of a differential reading structure and the use of enlarged transistors. However, the DCT7T design achieves a 22.64% reduction in read power consumption compared to the Conv6T design by employing a lower reading frequency (f). Even though the Conv8T, SE8T, and proposed SE6T SRAMs utilize a single-ended reading structure, the SE8T design incorporates an additional control signal (V_{GND}), leading to increased dynamic power consumption. When comparing the Conv8T and proposed SE6T SRAMs, the former demonstrates the lowest

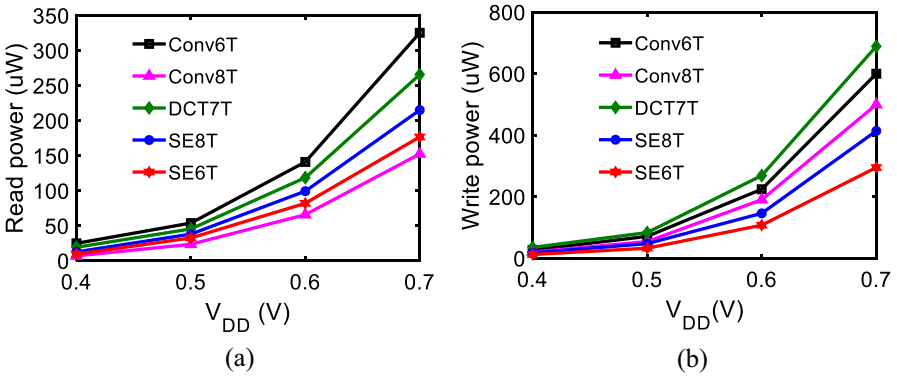


Fig. 13 Dynamic power for the investigated SRAMs versus V_{DD}, **a** Read power and **b** Write power

read power consumption due to the high read current in the proposed SE6T design, resulting in increased power consumption. At $V_{DD} = 0.4$V, the proposed SE6T design reduces read power consumption by 61.82%, 50.65%, and 25.43% compared to the Conv6T [23], DCT7T [17], and SE8T [30] SRAMs, respectively, and shows 1.36 × penalty in read power compared to the Conv8T [40].

Figure 13b illustrates a comparison of the write power consumption among the investigated SRAMs at different V_{DD} values. The Conv6T, DCT7T, and Conv8T designs exhibit higher write power consumption in comparison to the other SRAMs, primarily due to their utilization of a differential writing structure. The higher writing frequency (f) employed in the DCT7T design contributes to increased write power consumption. Moreover, the Conv6T design employs wider transistors than the Conv8T design, which further increases write power consumption. In contrast, the SE8T and proposed SE6T SRAMs, utilizing a single-ended writing scheme, demonstrate the lowest levels of write power consumption. However, the SE8T design displays higher write power consumption compared to the proposed SRAM due to the utilization of a columnar control signal (*WLB*). Furthermore, in the proposed SE6T design, the inverter M2-M4 is supplied by the *WBL* bitline, resulting in further reduction in write power consumption. At $V_{DD} = 0.4$V, the proposed SE6T design reduces write power consumption by 53.94%, 39.74%, 64.94%, and 31.02% compared to the Conv6T [23], Conv8T [40], DCT7T [17], SE8T [30] SRAMs, respectively.

5.6 Leakage Power

When evaluating an SRAM array, a significant portion remains in an idle state for prolonged durations in order to maintain the stored data [26]. Consequently, the dissipation of leakage power by an SRAM array becomes a crucial parameter that must be taken into consideration. To minimize the overall power consumption in an SRAM array, it is advantageous to design a low leakage power SRAM cell. The leakage power of an SRAM cell can be determined using Eq. (9) [29], where I_{SUB} is the subthreshold

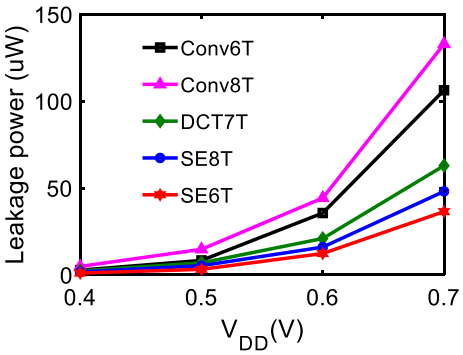


Fig. 14 Leakage power for the understudy SRAMs versus V_{DD}

leakage current.

$$P_{Leakage} = I_{Leakage} \times V_{DD} = (\sum_{i} I_{SUB,i}) \times V_{DD} \tag{9}$$

The leakage power dissipation for all the SRAMs studied in this research as compared to V_{DD} is illustrated in Fig. 14. Among them, the Conv8T exhibits the highest leakage power dissipation, primarily due to its utilization of a larger number of bitlines and the incorporation of a decoupled path for the read operation, which is the primary source of the leakage. Following that, the Conv6T and DCT7T SRAMs consume relatively higher leakage power when compared to the other SRAMs. This is attributed to their utilization of differential structures, along with enlarged transistors. However, the DCT7T exhibits lower leakage power dissipation compared to the Conv6T, which can be attributed to the inclusion of a diode-connected transistor (M7) in the pull-down networks of the cross-coupled structure of inverters. Both the proposed SE6T and SE8T SRAMs effectively mitigate leakage in their reading paths, thereby reducing the total leakage power. Notably, the proposed SE6T exhibits the lowest leakage power dissipation as it utilizes a lesser number of transistors and employs the *WBL* bitline to supply the pull-up network of the inverter M2-M4. As evident in Fig. 14, the proposed SE6T SRAM design significantly improves leakage power dissipation by 61.29%, 78.05%, 53.65%, and 39.33% in comparison to the Conv6T [23], Conv8T [40], DCT7T [17], SE8T [30] SRAMs, respectively.

5.7 Monte-Carlo Simulations on SRAM's Stability

Although an SRAM cell should prioritize fast operation and low power consumption, it is also essential for it to possess robustness and reliability against parametric variations. In order to evaluate the robustness and reliability of the analyzed SRAM cells under different parametric variations, we have conducted Monte-Carlo (MC) simulations using 1000 samples. The variations in channel length (L_{ch}), oxide thickness (T_{ox}), intertube space of CNT (S), and CNT's diameter (D_{CNT}), which are significant process variations, were assumed to follow independent normal Gaussian distributions with a 3σ range of $\pm$ 15% (σ: sigma) from their nominal values. Additionally, the variation

in supply voltage (V_{DD}) was considered to have a uniform distribution with a 3σ range of $\pm$ 10% from its nominal value. The necessary details for the MC simulations setup are clearly provided in Table 4.

The MC simulation results for RSNM and WSNM for all the analyzed SRAM cells at $V_{DD} = 0.4$ V are summarized in Tables 5 and 6, respectively. In these tables, variability is defined as the ratio between the mean and the standard deviation (std.) [10]. As observed in Table 5, the Conv6T and DCT7T SRAM cells exhibit higher RSNM variability compared to the other SRAM cells due to the presence of read-disturbance issues. On the other hand, the remaining SRAM cells demonstrate read-disturbance-free operation and consequently exhibit lower RSNM variability. Notably, the proposed SE6T SRAM cell shows a reduction in RSNM variability of 81.15%,

Table 4 MC simulation setup

Parameter	Nominal value	Distribution type	Change
L_{ch}	32 nm	Gaussian	$3\sigma = \pm 15\%$
T_{ox}	4 nm	Gaussian	$3\sigma = \pm 15\%$
D_{CNT}	1.4879 nm	Gaussian	$3\sigma = \pm 15\%$
S	20 nm	Gaussian	$3\sigma = \pm 15\%$
V_{DD}	0.4 V	Uniform	$3\sigma = \pm 10\%$

Table 5 MC simulation results of RSNM for the investigated SRAM cells at $V_{DD} = 0.4$ V

SRAM cell	Mean (mV)	Std. (mV)	Variability	Min. (mV)	Max. (mV)
Conv6T [23]	84.9	20.71	0.244	55.8	115.4
Conv8T [40]	169.4	14.2	0.084	149.7	187.4
DCT7T [17]	45.19	20.67	0.457	17.49	72.23
SE8T [30]	169.4	14.25	0.084	149.6	188.1
SE6T	172.9	7.912	0.046	159.3	187.7

Table 6 MC simulation results of WSNM for the investigated SRAM cells at $V_{DD} = 0.4$ V

SRAM cell	Mean (mV)	Std. (mV)	Variability	Min. (mV)	Max. (mV)
Conv6T [23]	173.1	40.29	0.233	152.8	199.1
Conv8T [40]	138.5	14.84	0.107	123.9	180
DCT7T [17]	219.2	13.49	0.062	167.3	230.4
SE8T [30]	188	15.09	0.080	165.8	211.6
SE6T	201.5	7.265	0.036	192.4	213.5

45.24%, 89.93%, and 45.24% compared to the Conv6T [23], Conv8T [40], DCT7T [17], SE8T [30] SRAM cells, respectively.

Table 6 indicates that the Conv6T and Conv8T SRAM cells display higher WSNM variability due to the absence of any write-assist techniques. The DCT7T SRAM cell, which incorporates a diode-connected transistor to weaken the pull-down network, exhibits lower variability compared to the aforementioned SRAM cells. Furthermore, the proposed SE6T SRAM cell reduces WSNM variability by 84.55%, 66.36%, 41.94%, and 55.00% compared to the Conv6T [23], Conv8T [40], DCT7T [17], SE8T [30] SRAM cells, respectively. These improvements can be attributed to the inclusion of an additional charging/discharging path for the storage node Q during the write operation.

5.8 Proposed SE6T Design; CNTFET vs. MOSFET

This section presents a comparative analysis between the MOSFET-based and CNTFET-based configurations of the proposed SE6T design. The proposed SE6T has been designed and simulated using HSPICE software with the predictive technology model (PTM)-high performance (HP) 32-nm MOSFET technology [20].

Figure 15a displays the read butterfly curves for both the MOSFET-based and CNTFET-based designs of the proposed SE6T SRAM cell, with $V_{DD} = 0.4$ V. It can be observed that the CNTFET design improves RSNM by 1.39 times. Additionally, Fig. 15b showcases the combined read and write butterfly curves for both designs at $V_{DD} = 0.4$ V, with the CNTFET design enhancing WSNM by 1.16 times. The CNTFET-based proposed SE6T SRAM cell demonstrates higher RSNM and WSNM compared to its MOSFET counterpart for all considered supply voltage values, as depicted in Fig. 16a and b, respectively.

Tables 7 and 8 present the MC simulation results of RSNM and WSNM for both the MOSFET-based and CNTFET-based proposed SE6T SRAM cell, respectively, with $V_{DD} = 0.4$ V. This analysis provides insights into how these technologies perform in

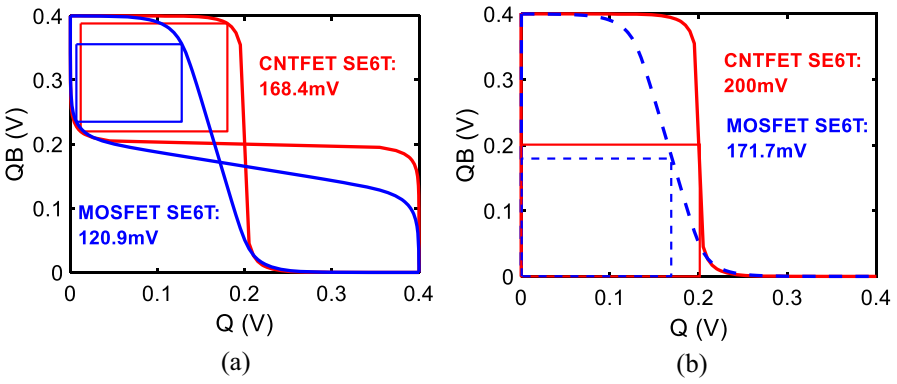


Fig. 15 A stability comparison between CNTFET- and MOSFET-based designs of the proposed SE6T SRAM cell at $V_{DD} = 0.4$ V, **a** Read butterfly curves and **b** Combined read/write butterfly curves

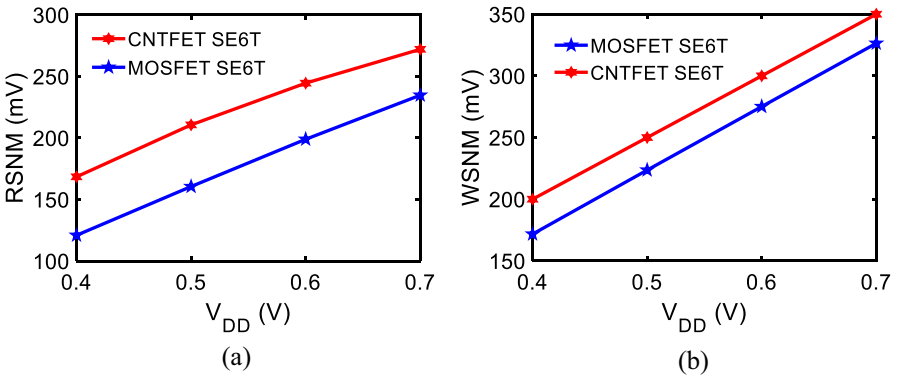


Fig. 16 A stability comparison between CNTFET- and MOSFET-based designs of the proposed SE6T SRAM cell versus V_{DD}, **a** RSNM and **b** WSNM

Table 7 MC simulation results of RSNM for the CNTFET- and MOSFET-based designs of the proposed SE6T SRAM cell at $V_{DD} = 0.4$ V

Design type	Mean (mV)	Std. (mV)	Variability	Min. (mV)	Max. (mV)
MOSFET	130.5	16.22	0.124	77.29	180.7
CNTFET	172.9	7.912	0.046	159.3	187.7

Table 8 MC simulation results of WSNM for the CNTFET- and MOSFET-based designs of the proposed SE6T SRAM cell at $V_{DD} = 0.4$ V

Design type	Mean (mV)	Std. (mV)	Variability	Min. (mV)	Max. (mV)
MOSFET	171.6	20.82	0.121	104.0	230.1
CNTFET	201.5	7.265	0.036	192.4	213.5

the presence of parametric variations. As observed in Tables 7 and 8, the CNTFET design shows improvements of 62.90% and 70.25% in RSNM and WSNM variabilities, respectively. This indicates that CNTFET technology exhibits lower sensitivity to parametric variations.

Table 9 documents the transient simulation results for both the MOSFET-based and CNTFET-based designs of the proposed SE6T SRAM at $V_{DD} = 0.4$ V. The CNTFET design offers notable improvements of 77.51%, 96.61%, 66.37%, 70.12%, and 74.83% in read delay, write delay, read power, write power, and leakage power, respectively. Consequently, CNTFET technology is more suitable for robust, stable, high-speed, and low-power SRAM designs.

Table 9 Delay and power comparison between CNTFET- and MOSFET-based designs of the proposed SE6T SRAM cell at $V_{DD} = 0.4$ V

SRAM metric	MOSFET-based SE6T	CNTFET-based SE6T	Improvement (%)
Read delay (ns)	2.89	0.65	77.24
Write delay (ns)	5.01	0.17	96.61
Read power (μW)	28.34	9.53	66.37
Write power (μW)	41.67	12.45	70.12
Leakage power (μW)	4.29	1.08	74.83

Table 10 Area estimation for the investigated SRAM bitcells

	The area (nm) of each transistor used								
SRAM bitcell	M1	M2	M3	M4	M5	M6	M7	M8	Total area (nm)
Conv6T [23]	41.49	1.49	41.49	1.49	21.49	21.49	*	*	128.94
Conv8T [40]	1.49	1.49	1.49	1.49	21.49	21.49	1.49	1.49	51.92
DCT7T [17]	41.49	1.49	41.49	1.49	21.49	21.49	41.49	*	170.43
SE8T [30]	1.49	1.49	1.49	1.49	1.49	1.49	1.49	21.49	31.92
SE6T	1.49	1.49	1.49	1.49	1.49	21.49	*	*	28.94

5.9 Area Estimation

The total area of the proposed SE6T SRAM bitcell and the other examined SRAM bitcells is computed by aggregating the areas of individual transistors within the circuits [35]. Table 10 provides an overview of the transistor areas utilized in the SRAM bitcells, as well as the overall area. As indicated by the data in Table 10, the proposed SE6T SRAM bitcell exhibits the smallest area, achieving notable improvements of 77.56%, 44.26%, 83.02%, and 9.34% compared to the Conv6T [23], Conv8T [40], DCT7T [17], and SE8T [30] SRAM bitcells, respectively.

5.10 Half-Select Issue Elimination

The proposed SE6T SRAM cell design was illustrated in Fig. 3, features a row-based control signals *WWL* and V_{GND}. During a standard write operation in a selected SRAM bitcell, these row-based signals may impact all bitcells within the same row. Consequently, it can be inferred that the entire row is written in the proposed SE6T SRAM

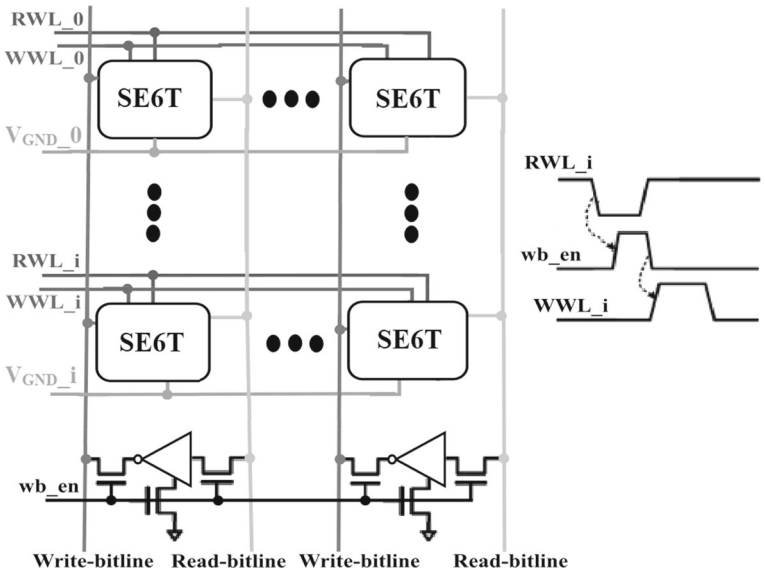


Fig. 17 The scheme (presented in [28]) to eliminate the row half-select disturbance issue in a write operation

cell structure, as described in [1]. If this is not the case, the half-select-disturbance issue can be mitigated through the power-efficient write-back circuit proposed in [28].

The write-back technique involves a multi-step process. Initially, the read wordline for the specified row (*RWL_i*) is activated, allowing the data from half-select cells in that row to be sensed through their read-bitlines. The read data is then written back to the corresponding write bitlines via a combination of three n-type transistors and an inverter, controlled by the *wb-en* signal, as depicted in Fig. 17. Subsequently, *wb-en* is deactivated, and the embedded inverters are disconnected from the read/write bitlines to prevent interference with the normal operation of the SRAM array. Furthermore, the transistor located at the bottom of the embedded inverters is placed in a non-conductive state to prevent short/leakage current flow during idle periods. Finally, the corresponding write wordline (*WWL_i*) is activated.

During the write operation, the stored charges on the write bitlines do not compromise the internal voltages of half-select cells, as the bitline voltages are identical to the internal node voltages, thereby resolving the half-select-disturb issue. This technique does not necessitate the full process of read and write operations, as proposed in [28], and thus exhibits reduced power consumption.

The employed internal write-back scheme benefits from two advantages, which result in improvements in the proposed SRAM performance [28]:

- The full process of read operation including activation of the word line signals, sense amplifiers, latches and so on is not done.
- The full process of the write operation is not necessary. Since we just want to change the voltage of the bitlines during the write-back operation, less effort is needed and a small inverter is enough.

In modern microprocessors, a sequence of 10–50 consecutive write operations is common [28]. With the internal write-back scheme, partial-read and write-back processes are necessary only for the first operation in these sequences. This leads to a reduction in delay and power overheads, cutting them to at least 10% of their current levels. For our evaluation of the proposed design's power performance, we analyze a scenario with 10 consecutive write operations, comparing it to the conventional 6T design. Both designs are assessed at a size of 4Kb (64 × 64). At a V_{DD} of 0.4 V and room temperature, the proposed design shows a power consumption of 1.28 mW for these ten write operations, which is 16.34% lower than that of the conventional 6T design.

We utilize a differential cross-coupled sense amplifier instead of a single-ended inverter to enhance read speed and reduce power consumption during access. This design allows the readout circuitry to detect small voltage differences even before sneaking currents emerge. Compared to inverter-based sensing, the differential cross-coupled sense amplifier improves read speed by 30% through small signal sensing and reduces power consumption by 25% by eliminating sneaking and short-circuit currents [14]. Additionally, we generate a pulsed row *RWL*, enabling the selected *RWL* for a shorter duration (Fig. 4b). This approach effectively terminates the sneak current path as soon as the *RWL* is disabled [22].

Since the internal write-back scheme was used to prevent data-missing in cells located in the same row, we have measured the SNMs of the row half-selected bitcells at $V_{DD} = 0.4$ V for before and after applying the internal write-back technique. As shown in Fig. 18, the row half-selected SRAM bitcells offer HSNM and RSNM equal to 168 mV, which are same for with and without internal write-back technique. This is because the proposed design experiences data-missing while performing a write operation. On the other hand, after applying internal write-back technique, the value of WSNM reaches 70 mV (8.75 times improvement). This value is enough to maintain the data during normal operation in the selected SRAM bitcell.

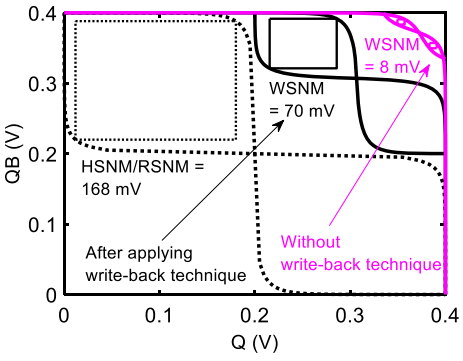


Fig. 18 SNMs of the row half-selected SRAM bitcells at $V_{DD} = 0.4$ V for before and after applying internal write-back scheme

5.11 Summary of Results

All the simulation results obtained in this study, along with the primary characteristics, of the investigated SRAM cells, including Conv6T [23], DCT7T [17], Conv8T [40], SE8T [30], and proposed SE6T, are documented in Table 11. The aforementioned SRAM cells have been simulated using the HSPICE simulator with the Stanford University 32-nm CNTFET technology [14, 15, 35] at $V_{DD} = 0.4$ V. According to Table 11, the proposed SE6T demonstrates the highest HSNM and RSNM, the second-highest WSNM, as well as the lowest RSNM and WSNM variabilities. It also exhibits the second-lowest read delay and read power. The proposed SE6T possesses a write delay that is relatively high due to its single-ended writing structure, but it consumes the least amount of write power. The leakage power dissipated by the proposed SE6T is the lowest compared to the other SRAMs under investigation. Additionally, the estimated area of the SRAM bitcell, based on its total width, is the lowest for the proposed SE6T SRAM bitcell since it utilizes five CNTFETs with one CNT and one CNTFET with two CNTs.

Table 11 Features and simulation results for the investigated SRAM cells

Features & Metrics	Conv6T [23]	DCT7T [17]	Conv8T [40]	SE8T [30]	SE6T (prop.)
V_{DD} (V)	0.4	0.4	0.4	0.4	0.4
Technology node (nm)	32	32	32	32	32
Device	CNTFET	CNTFET	CNTFET	CNTFET	CNTFET
No. transistors	6	7	8	8	6
No. bitlines	2	2	3	2	2
No. signals	1	1	2	4	3
Read/Writing structure	Diff./Diff	Diff./Diff	SE/Diff	SE/SE	SE/SE
Read disturb free	No	No	Yes	Yes	Yes
HSNM (mV)	165.1	133.1	168.4	167.6	168.4
RSNM (mV)	84.6	53.1	168.4	167.6	168.4
WSNM (mV)	158.2	229.5	138.2	177.9	200
RSNM variability	0.244	0.457	0.084	0.084	0.046
WSNM variability	0.233	0.062	0.107	0.080	0.036
Read delay (ns)	0.40	3.01	0.85	0.94	0.65
Write delay (ps)	107.65	101.91	102.87	195.28	167.64
Read power (μW)	24.96	19.31	7.01	12.78	9.53
Write power (μW)	27.03	35.51	20.66	18.05	12.45
Leakage power (μW)	2.79	2.33	4.92	1.78	1.08
Area (total width) (nm)	128.94	170.43	51.94	31.92	28.94

6 Conclusion

This paper presented a CNTFET-based robust, low-power SRAM cell consisting of six transistors, with high read stability and writability. The simulation results demonstrated that the proposed SE6T design improved RSNM by 1.99 × /3.17 × and enhanced WSNM by 1.26 × /1.45 × /1.12 × compared to Conv6T/DCT7T and Conv6T/Conv8T/SE8T, respectively. It also reduced RSNM/WSNM variability by at least 45.24%/41.94%. The read delay and write delay in the proposed SE6T SRAM are reduced by 85.80%/24.19%/25.40% and 16.15 in comparison with DCT7T/Conv8T/SE8T and SE8T, respectively. In terms of power efficiency, the proposed SE6T design reduced read power by 61.82%/50.65%/25.43% compared to Conv6T/DCT7T/SE8T. The write power and leakage power are improved by at least 31.02%/39.33%, correspondingly. All these improvements were at the expense of 1.15 × lower WSNM compared to DCT7T, 3.92 × higher read delay compared to Conv6T, 1.56 × /1.64 × /1.63 × higher write delay compared to Conv6T/DCT7T/Conv8T, and 1.36 × higher read power compared to Conv8T. The simulation results demonstrated that the CNTFET design offers notable improvements of 77.24%, 96.61%, 66.37%, 70.12%, and 74.83% in read delay, write delay, read power, write power, and leakage power, respectively than MOSFET design. The CNTFET design also increased RSNM/WSNM by 1.39 × /1.16 × and reduced RSNM/WSNM variability by 62.90%/70.25% than MOSFET design.

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Data Availability The data will be shared on request to the corresponding author.

Declarations

Conflict of interest (a) The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. (b) Authors confirm that they have no conflict of interest as well as no financial interests related to work submitted for possible publication in this Journal. The data generated and analyzed during this study are available from the corresponding author on reasonable request.

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