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A new H6 neutral point clamped transformerless photo voltaic inverter

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Transformerless photovoltaic (PV) inverters are widely used in grid-connected solar energy systems due to their high efficiency and compact design. However, conventional transformerless inverters suffer from oscillating common-mode voltage (CMV), which leads to higher common-mode leakage current (CM-LC) due to the lack of galvanic isolation. This issue adversely affects system performance, safety, and compliance with grid standards. To address these challenges, this paper proposes a novel H6 Neutral Point Clamped (NPC) transformerless inverter topology, termed the H6-Diode (H6-D) topology, which integrates the advantages of AC-bypass low-loss switching and common-mode leakage current (CM-LC) elimination. The proposed topology features a clamping circuit that restricts the freewheeling voltage to half of the DC-link voltage, effectively minimizing CM-LC. The theoretical framework of the proposed design is rigorously validated through comprehensive simulations in MATLAB/Simulink and experimental verification using a laboratory prototype. The performance of the proposed inverter is evaluated based on key criteria, including common-mode voltage (CMV), common-mode leakage current (CM-LC), total harmonic distortion (%THD), switching and conduction losses, and overall efficiency. Compared to recent transformerless inverter topologies, the proposed H6-D topology demonstrates superior performance, achieving higher efficiency, lower THD, reduced voltage stress across components, and effective suppression of CM-LC. These results highlight its potential as a promising solution for high-performance grid-connected photovoltaic (PV) applications.

Keywords Transformer-less inverter, Common mode voltage, Leakage current, Non-NPC, NPC inverter, Total harmonic distortion, Efficiency

Photovoltaic (PV) energy is highly valued for its eco-friendly attributes and its growing role in renewable energy solutions. In grid-connected PV applications, inverters are crucial for energy conversion and can be classified as either with or without transformers. Inverters with transformers face limitations of their bulky size, weight, higher cost and power losses as well[1,2]. To overcome these limitations, transformer-less photovoltaic inverters (TL-PVIs) have been developed and are gaining significant attention across various fields[4,5]. However, TL-PVIs also present some technical challenges, primarily due to the lack of galvanic isolation between the PV system and the grid. This lack of isolation can lead to dangerous common mode leakage currents (CM-LCs) in the resonance circuit parameters, which affect current ripples, human safety, and cause electromagnetic interference (EMI) problems[2–4]. According to the VDE-AR-N 4105 standard, PV panels must disconnect from the grid if the leakage current exceeds 300mA[3].

Thus, eliminating CM-LCs has become a critical issue in distributed PV systems. Various solutions have been proposed to address CM-LC issues, focusing on two main approaches. The first approach involves creating a freewheeling current path to reduce CM-LC by separating the grid from PV arrays referred as non-neutral-point-clamped method (non-NPCM). The second approach incorporates an additional clamping branch to

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maintain a stable common-mode voltage (CMV) with low common-mode leakage current (CM-LC), commonly known as the neutral-point-clamped method (NPCM)[4–6]. In recent advancements, super-junction metal-oxide-semiconductor field-effect transistors (SJ-MOSFETs) have been adopted as power devices to enhance the efficiency of photovoltaic (PV) systems. However, SJ-MOSFETs exhibit significant reverse recovery issues, which can lead to shoot-through effects between upper and lower complementary switches, thereby complicating the design of transformerless photovoltaic inverters (TL-PVIs)[7,8]. To address these challenges, various topologies have been developed using MOSFETs as the primary power devices to achieve optimal European (EU) efficiency[9,10].For example, SMA proposed a non-NPC H5 topology by adding a one more switch between the DC side of the PV panel and the H4 circuit legs[11]. Similarly, Sunway introduced the "Highly Efficient and Reliable Inverter Concept" (HERIC) for high-efficiency applications, featuring a freewheeling branch with two IGBTs (S5 and S6) and four MOSFETs (S1-S4) to achieve higher EU efficiency[12], as shown in Fig. 1(a). However, non-NPC topologies like H5 and HERIC are not ideal for PV applications due to poor common-mode behavior throughout the grid cycle. In conclusion, while TL-PVIs offer a promising solution for efficient and eco-friendly energy conversion in PV systems, addressing CM-LC issues and optimizing inverter designs remain critical areas for ongoing research and development.

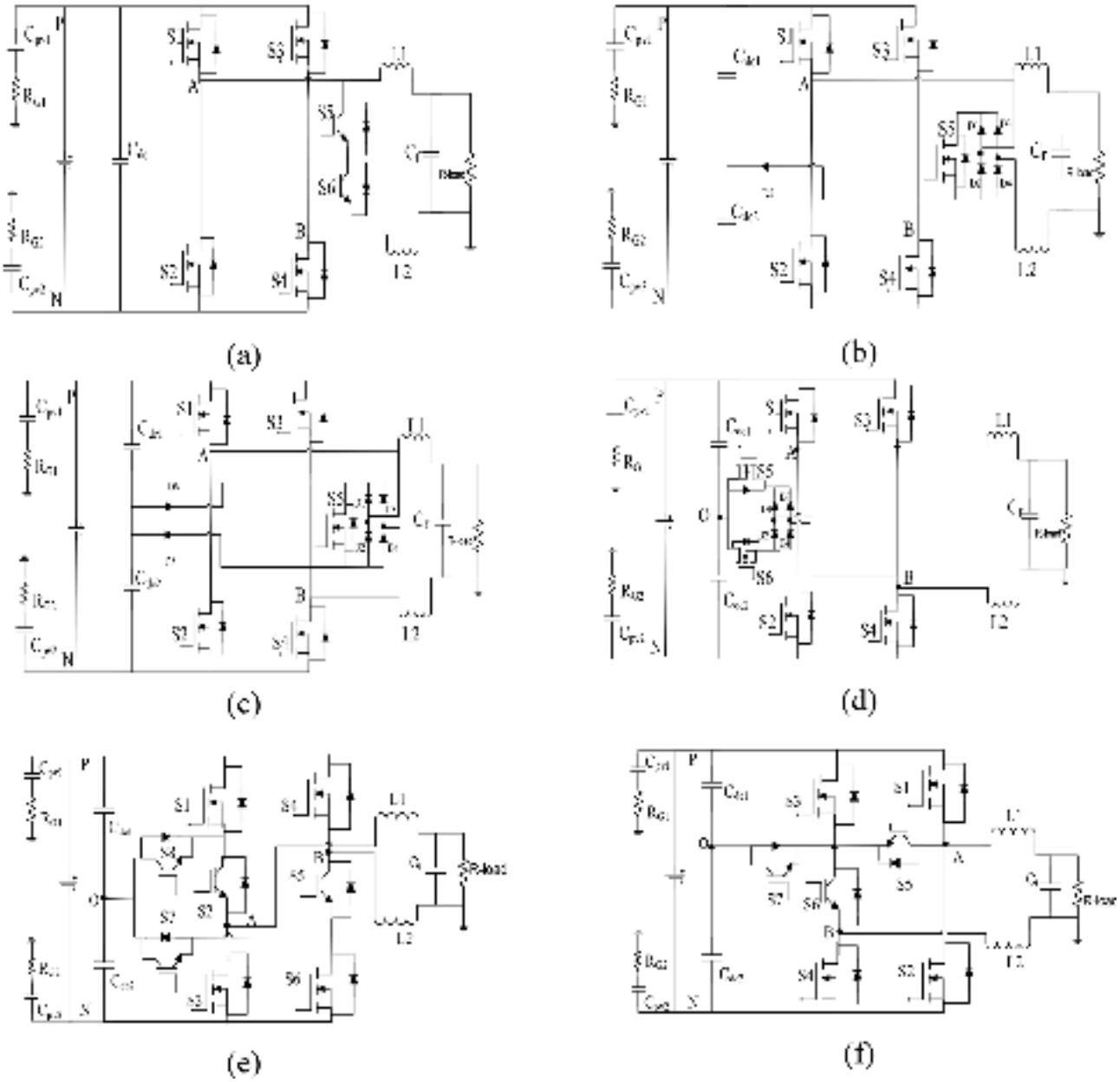


Fig. 1. Existing single-phase TL-PVI topologies: (**a**) Heric (**b**) HBZVR, (**c**) HBZVR-D, (**d**) HBZVSCR, (**e**) PN-NPC and (**f**) H6-1.

On the other hand, NPCM topologies combine the benefits of galvanic isolation and common-mode (CM) clamping[16–18]. For instance, a rectifier bridge type topology namely HBZVR introduced with rectifier bridge circuit such as one active S5 switch and four diodes (D1-D4) at DC-link midpoint across the capacitor, as illustrated in Fig. 1(b)[13]. However, it struggles to maintain a constant CMV due to inadequate clamping during freewheeling periods. To report this issue, an additional diode was introduced in the HBZVR-D topology, which shown in Fig. 1(c)[14]. This modification ensures CMV constant and leakage current elimination throughout the entire grid cycle. Recently, another variant called the rectifier bridge type topology namely HB-ZVSCR was proposed to enhance common-mode characteristics depicted in Fig. 1(d)[15]. Similarly, positive-negative NPC (PN-NPC) and H6-family TL-PVI topologies have been developed, featuring a bidirectional active CM-clamping section presented in Fig. 1(e) and (f)[16–20]. These topologies clamp half of the DC input voltage, effectively eliminating CM-LC. However, they suffer from relatively higher losses due to the increased number of switches (S2, S5, S7 and S8) involved during freewheeling periods.

From these discussions, it is clear that while galvanic separation is crucial, it alone cannot entirely eliminate CM-LC due to device junction and stray capacitance influence on the system[18–20]. Further advancements in topology design and component optimization are necessary to fully address CM-LC issues and improve the performance of TL-PVIs. Another noteworthy topology, known as the oH5, utilizes a CM-active clamping technique as detailed in[17]. In this design, one more switch is added at the center-point of the DC-link capacitor and bridge arms to maintain a constant CMV. However, this topology fails to achieve constant CMV during dead time periods. An elegant H6 topology, introduced in[20], incorporates two active switches and two passive diodes at DC-link midpoint and bridge arms. This configuration addresses some of the CMV issues but still faces challenges. In addition to the aforementioned challenges, the HBZVR, H6-type also faces limitations concerning shoot-through on the DC link in non-NPC topologies. The use of IGBTs as the main switch in this configuration further hampers performance, resulting in lower European (EU) efficiency compared to other designs. This is primarily due to the inherent characteristics of IGBTs, which generally have higher switching losses and slower response times compared to MOSFETs. The Heric topology has also seen improvements with the introduction of the Oheric inverter, as discussed in[22–23]. Its design includes two additional active IGBT devices (S7 and S8) at the center-point of the DC-link capacitor, which enhances CM behavior and reduces CM-LC. Nevertheless, the H6 and Oheric configurations, while effective in managing CM issues and reducing leakage currents but due to more active switches in freewheeling periods it from higher conduction losses.

Additionally, other high-efficiency clamped topologies such as I-NPC and T-NPC type half-bridge inverters have been proposed in[24–25]. In the I-NPC design, clamping circuits are constructed using two passive diodes, whereas the T-NPC designed by the bidirectional active devices at the center-point of the DC-link capacitor. These designs require operation at double the input DC voltage ($2V_{dc}$) in full-bridge circuits[26,28,29]. In the literature, another notable H6-type MOSFET solution is proposed in[27–30,31], which claims excellent control of common-mode voltage (CMV) and effectively reduces leakage currents. However, it suffers from the drawback of requiring large components during freewheeling periods, which leads to increased losses. In summary, while various topologies referred as HBZVR, HBZVR-D, HBZVSCR, oH5, H6-Ttype1, H6-type2, Oheric, PN-NPC, I-NPC, and T-NPC offer solutions to manage CMV and reduce leakage currents, each has trade-offs in terms of efficiency, complexity, and switching losses[32–34]. Ongoing research and innovation are essential to optimize these designs for better performance and reliability in PV applications[35–37].

Based on the H6-type with NPCM, a new H6 MOSFET topology is introduced to unify the ac-bypass low loss scheme with the common mode leakage current eradication capabilities of the clamping method referred as H6-D neutral point clamped inverter. This topology aims to address several critical issues in photovoltaic inverter design while enhancing overall performance.

The key features of the H6-D topology are highlighted below:

- CMV is constant at $0.5V_{dc}$ and CM-LC is eliminated, close zero.
- Shoot-through issues are suppressed.
- No reverse recovery loss.
- Overall losses reduced significantly.
- Lower switching stress across the clamping circuit elements.
- Enhanced European (EU) efficiency.

This H6-D MOSFET inverter offers a comprehensive solution by merging the best features of low-loss and leakage current elimination methods, paving the way for more efficient and reliable photovoltaic energy systems. Additionally, the H6-D topology is capable of reactive power generation during in non-unity power factor, which is a crucial feature for future transformer-less photovoltaic inverter (TL-PVI) topologies. The performance comparison of proposed new H6-D topology among other non-NPC (Heric, HBZVR) and NPC (HBZVSCR, PN-NPC, H6-1) TL-PVI topologies are evaluated in terms of common-mode-voltage (CMV), CM-leakage current, total harmonic distortion (%THD), loss analysis, switching stress and efficiency respectively. These comparisons are conducted through simulations and verified further with experimental tests.

This article is systematized as follows; in Sect. "Proposed H6-type neutral-point-clamped topology" discussed the proposed H6-D topology description, principles and its modes of operations as well. Simulation and loss evaluations are framed in Sect. "Simulation results" and experimental results confirming the theoretical and simulation findings are contributed in Sect. "Experimental results" At the end summarizes the elicited results and concludes the article in Sect. "Conclusion".

Proposed H6-type neutral-point-clamped topologyy

Description of H6-D MOSFET topology and modulation method strategy

Based on the above discussions, a new H6 configuration is proposed with SJ-MOSFETs as main power devices to merge the features of the ac-bypass low-loss technique and NPCM to eliminate the common mode-leakage-current. Its topological source derivations are presented in[21], which results in the failures of the gate drive circuit (shoot-through) being reduced significantly and thus enhanced system reliability and efficiency as well. Both point legs (A, B) across the DC-link are coupled with two identical inductors either L1 or L2. The proposed new H6-D consists of a five switches (S1 – S5) and the CM clamping section is realized with a trivalent rectifier bridge with one switch (S6), four diodes (D1-D4), and freewheeling path current is provided via D_5 and D_6 at mid-point of the DC-link capacitors, as shown in Fig. 2(a).

The proposed H6-D topology employs a modified unipolar sinusoidal pulse-width modulation (SPWM) technique, specifically tailored to align with the inverter's structural design. This modulation approach facilitates the coordinated operation of the active switches and clamping circuit, ensuring the advantages of AC-bypass low-loss switching and effective suppression of common-mode leakage current (CM-LC). Additionally, the strategy is optimized to lower switching losses, minimize voltage stress, and maintain low total harmonic distortion (THD), enhancing the overall performance of the inverter.

The chosen modulation method was selected after a comprehensive analysis and comparison with alternative techniques, including bipolar SPWM and hybrid modulation. The unipolar SPWM approach proved to be the most effective for the H6-D topology due to the following advantages:

- Ensures smooth operation of the clamping circuit, limiting freewheeling voltage to half of the DC-link voltage.
- Reduces switching losses by minimizing the number of switching transitions.
- Effectively suppresses CM-LC by maintaining a stable common-mode voltage (CMV).

Operating principles of the proposed new H6-D TL-PVI topology

The switching scheme of the H6-D TL-PVI with Unity PF is demonstrated in Fig. 2(b). Here the G1 to G6 are the modulating signals for the S1 to S6 respectively. And S6 is switched at grid frequency in the whole grid periods.

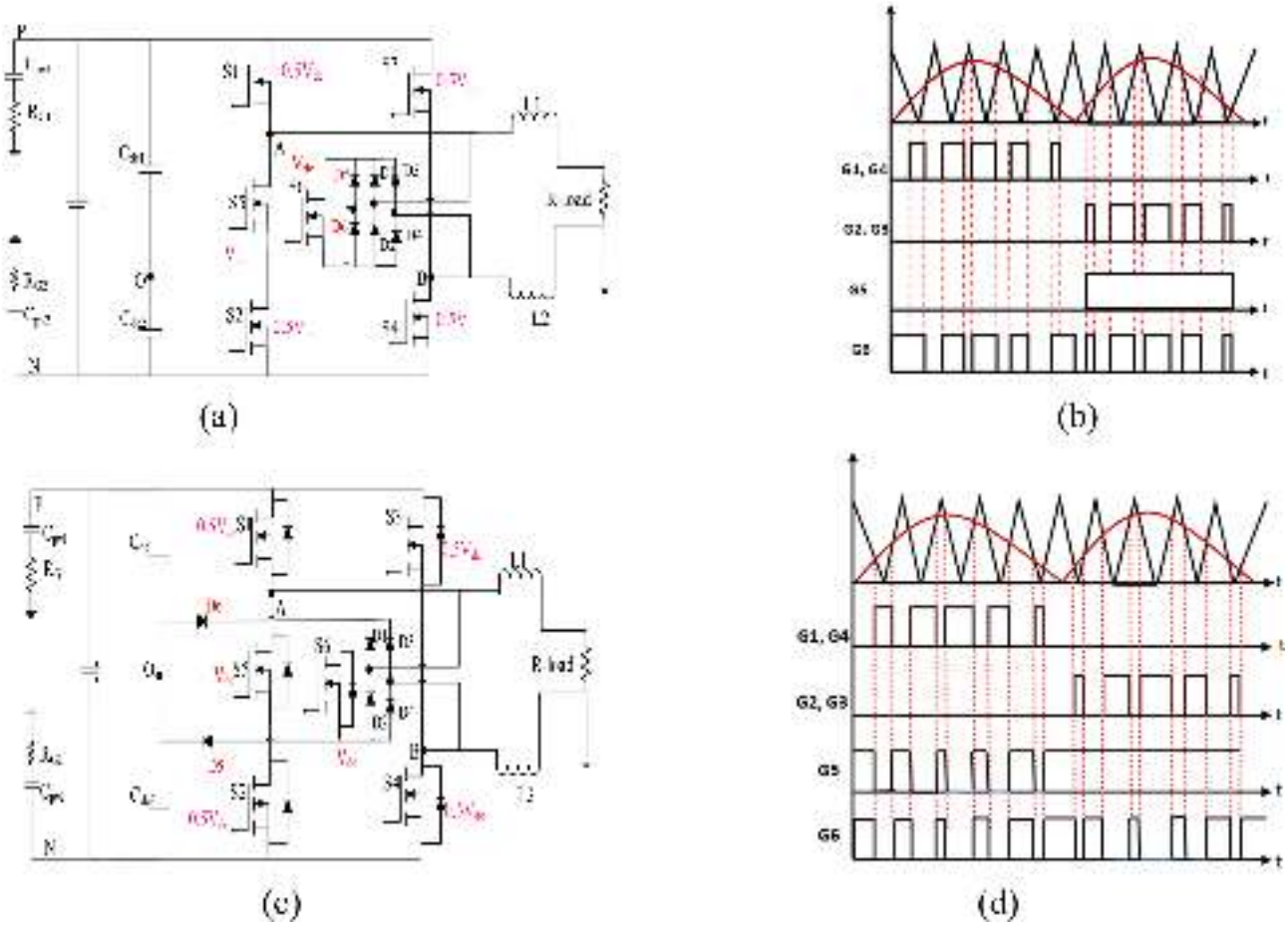


Fig. 2. Proposed novel H6-D topologies. (**a**) circuit Structure (**b**) unity power factor gate pulses, (**c**) Variant of H6-D, (**d**) Non unity power factor gate signals.

Similarly, variant of proposed H6-D topology and corresponding gate pulse pattern at non-UPF, as shown in Fig. 2(c-d), where MOSFET body diodes are active and hence limited applications. The operating modes for the.

H6-D TL-PVI with three-level output voltages (+ V_{PV}, 0, and -V_{PV}) are described in Fig. 3. The detailed switching modes, CMV and DM evaluations on non-NPC and NPC topologies are presented in Table 1[2].

In mode 1 which is the active positive half-period stage (APHPS), two switches S1, S4 are tuned on and others are switched off. The current rises linearly and flows via S1, load, S4, as illustrated in Fig. 3(a).

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{dc} + 0) = \frac{V_{dc}}{2} \tag{1}$$

$$V_{AB} = V_{AN} - V_{BN} = V_{dc} - 0 = V_{dc} \tag{2}$$

In mode 2, during the positive half freewheeling period (PHFP) dc source is completely isolated from the grid. In this mode, S6 is switched on while the remaining switches are turned off. As depicted in Fig. 3(b), the current freewheels through D2, D3, S6, and D5, causing the inductor current to decrease accordingly. During this stage, the voltage values change: V_{AN} decreases and V_{BN} increases until they reach $0.5V_{dc}$ or become equal. Consequently, the freewheeling voltage is

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\right) = \frac{V_{dc}}{2} \tag{3}$$

$$V_{DM} = \frac{V_{dc}}{2} - \frac{V_{dc}}{2} = 0 \tag{4}$$

In mode 3 it is active negative period stage (ANHP), the two switches S1, S3 are tuned on and others are switched off. During this stage current freewheels via S4, load, S3 and S5, as shown in Fig. 3(c).

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(0 + V_{dc}) = \frac{V_{dc}}{2} \tag{5}$$

$$V_{DM} = 0 - V_{dc} = -V_{dc} \tag{6}$$

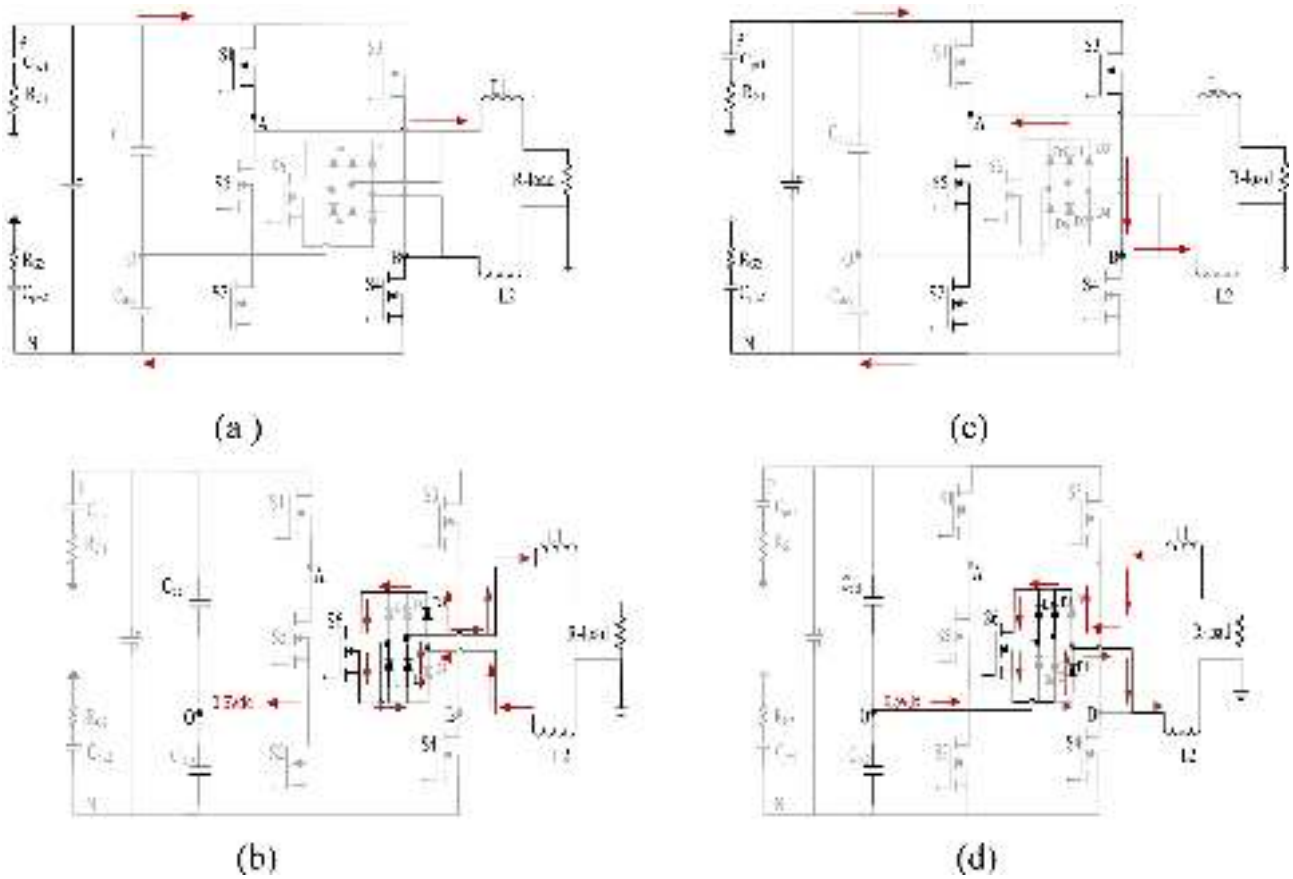


Fig. 3. Operating modes for the H6-D TL-PVI: (**a**) Active conduction period. (**b**) Active freewheeling in positive half period (PHP). (**c**) Active conduction and (**d**) Active freewheeling in negative half period (NHP).

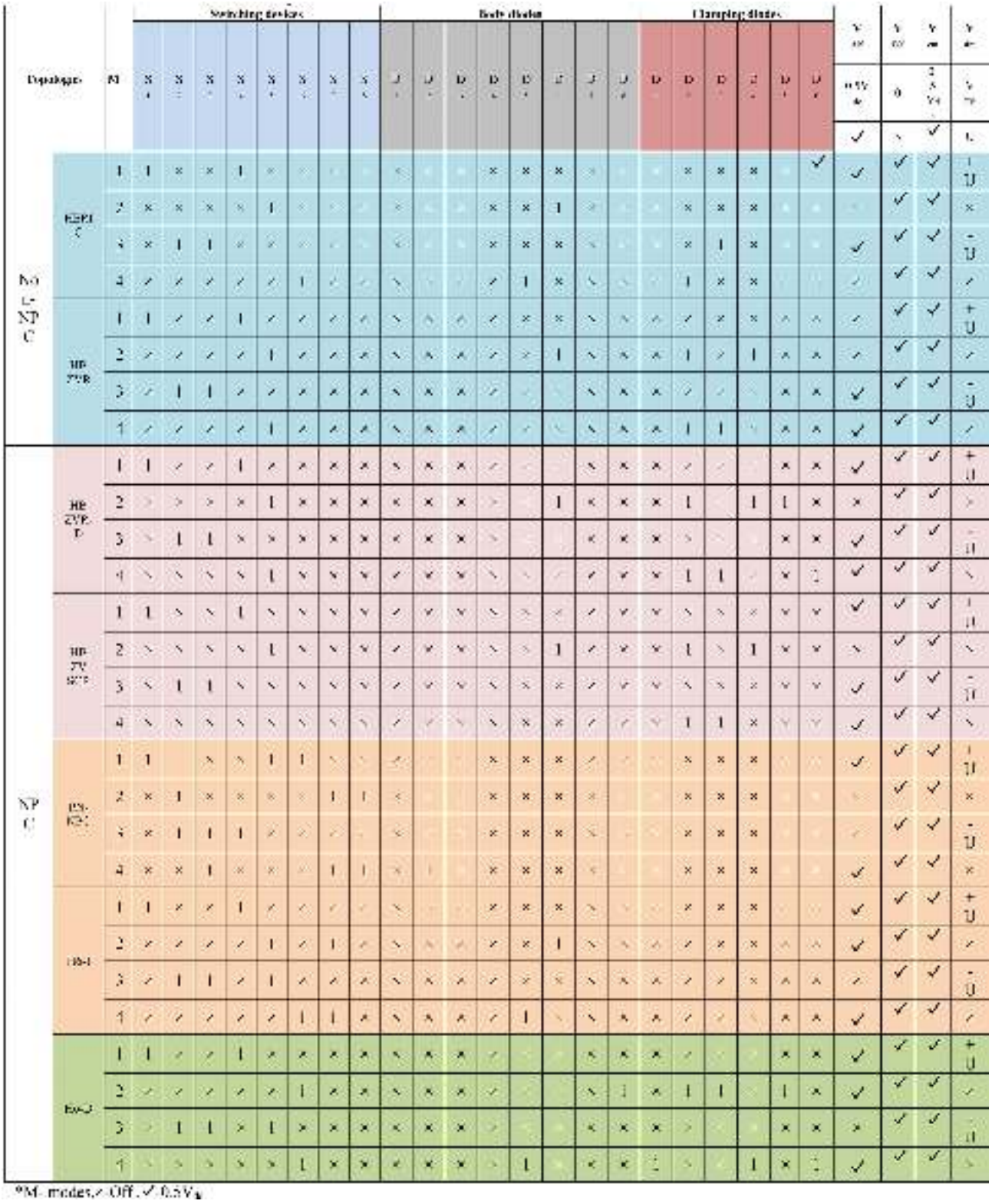


Table 1. Switching Modes, CMV And DM Evaluations On Non-NPC And NPC Topologies.

In mode 4, during the negative half freewheeling period (NHFP) dc source is completely isolated from the grid. In this mode, S5, S6 are switched on while the remaining switches are turned off. As depicted in Fig. 3(d), the load current freewheels through D6, S6, load, D1 and D4, causing the inductor current to increases accordingly. During this stage, the voltage values change: V_{AN} increases and V_{BN} decreases until they reach $0.5V_{dc}$ or become equal. Consequently, the freewheeling voltage is

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\right) = \frac{V_{dc}}{2} \tag{7}$$

$$V_{DM} = \frac{V_{dc}}{2} - \frac{V_{dc}}{2} = 0 \tag{8}$$

However, during the freewheeling modes, the potential of freewheeling path (P_{FP}) is operated in two ways such as if $P_{FP} > V_{dc}$ then clamping diode D_5 is active to carry the current to fixed at constant CMV and $P_{FP} < V_{dc}$ then clamping diode D_6 active to flow the current to fixed at constant CMV across the centre-point of dc-link. On the other hand, in the proposed H6-D, the extra switch (S6) is helpful during the freewheeling modes such as to clamp the DC input voltage at $0.5V_{dc}$ under abnormal conditions and also reactive power generation as well in future-generation inverters. From the discussions, it is noticed that mode1 to mode4 constant CMV achieved due to improved clamping branch in the freewheeling periods. Therefore, the CM-LC is completely eliminated[20]. It is clearly shown that the MOSFETs body diodes are absent in the whole grid cycle. To prevent body diode conduction and eliminate reverse recovery losses, the proposed H6-D topology is designed to operate at unity power factor (PF = 1). At non-unity PF, reactive power causes current reversals, activating MOSFET body diodes, which leads to reverse recovery losses. By maintaining unity PF, the current stays in phase with the voltage, preventing body diode conduction. The unipolar SPWM modulation used in the H6-D topology ensures smooth switching transitions, avoiding freewheeling through body diodes. Additionally, the clamping branch keeps the common-mode voltage (CMV) stable, further preventing diode activation. As a result, the H6-D topology eliminates reverse recovery losses, improving overall efficiency and reliability in transformerless PV inverters.For this reason, H6-D is made with MOSFETs as main power devices without any surplus issues. Moreover, in H6-D all MOSFETs are working at lower voltage rating, which is compared with other non-NPC and NPC topologies, and it will be discuss in the next section. It makes proposed new H6-D topology is most worthy for high efficiency PV applications.

Simulation results

Here proposed topology is tested and compared with other non-NPC and NPC configurations through simulation studies. The parameters used in these simulations include an input DC voltage of 400 V, parasitic capacitors (C_{PV1} and C_{PV2}) of 100nF, and ground resistances (R_{G1} and R_{G2}) of 11Ω. Additionally, the system features two identical filter inductors (L1 and L2) rated at 3mH, and a switching frequency of 10 kHz[4]. These parameters provide a origin for evaluating the performance of the H6-D topology against other configurations, with a focus on key metrics such as common-mode voltage (CMV), common mode leakage current (CM-LC), total harmonic distortion (THD), loss analysis, and efficiency.

Performance of output characteristics and common-mode results

Figures 4 and 5 illustrate the simulation results, showcasing the output characteristics (V_{out}, I_{out}, i_{leak}) and the common-mode characteristics (V_{AN}, V_{CM}, V_{BN}) of non-neutral-point-clamped and NPC topologies. The results demonstrate that all topologies achieve a 3-level output voltage ($+V_{pv}$, 0, $-V_{pv}$) and produce output current in a sinusoidal behaviour. However, the HERIC has poor common-mode behavior, which is not meet theoretical expectations, particularly with floating phase-leg voltages (V_{AN}, V_{BN}), leading to a common-mode voltage (CMV) that oscillates around ~220 V, as depicted in Fig. 5(a). mode voltage (CMV) to oscillate around ~230 V, as shown in Fig. 5(b). This oscillation leads to a significant increase in common-mode leakage current, as depicted in Fig. 4(b). The poor clamping behavior during freewheeling periods is a key factor contributing to this issue.

Therefore, the common mode leakage current is not limited to suppress, which is displayed in Fig. 4(a). However, the HBZVR exhibits worst common-mode performance, despite the use of a clamping section. The presence of spikes in the voltages $V_{AN,}$ V_{BN} and causes the common-. It has been demonstrated that neither galvanic isolation nor PWM methods alone can generate a constant CMV. Consequently, the HBZVR is categorized under the non-NPC category, exhibiting similar behavior to the HERIC topology. The aforementioned issues are overcome by NPC configurations such as HBZVR-D, HBZVSCR, PN-NPC, H6-1 such as demonstrate excellent common-mode performance, maintaining constant phase-leg voltages (V_{AN}, V_{BN}) and a constant CMV at 200 V, as illustrated in Fig. 5(c-f). Consequently, common mode leakage current is successfully eliminated to zero in presented in Fig. 4(c-f). The proposed H6-D topology shows enhanced common-mode performance in the clamping branch, as seen in Fig. 5(g). In this topology, no voltage spikes are observed in V_{AN} and V_{BN}, since they are complementary to each other. Consequently, the common-mode voltage (CMV) remains constant at 200 V across all periods, which completely eliminates the common-mode leakage current such as close zero, as depicted in Fig. 4(g).

To substantiate the claim of the voltage stress across the switches as well as zero reverse recovery losses in the MOSFET body diodes, the corresponding waveforms are presented in Fig. 6. Figure 6(a) illustrates the voltage stress across all six switches in the proposed H6-D topology. Four switches (S1, S2, S3, S4) operate at half of the DC-link voltage (0.5Vdc), while the remaining two (S5, S6) experience the full DC-link voltage (Vdc). This arrangement effectively reduces voltage stress on most switches, enabling the use of lower voltage-rated MOSFETs. Similarly, Fig. 6(b) presents the drain-source current of the MOSFET body diodes to verify the absence of reverse recovery losses in the proposed H6-D topology. The waveform clearly shows that there are no negative transitions or spikes in the body diode current of any switch, confirming the elimination of reverse recovery losses. Consequently, the reduction in switching losses leads to improved efficiency and enhanced overall reliability of the inverter, making the H6-D topology a highly efficient solution for low-voltage applications Table 2.

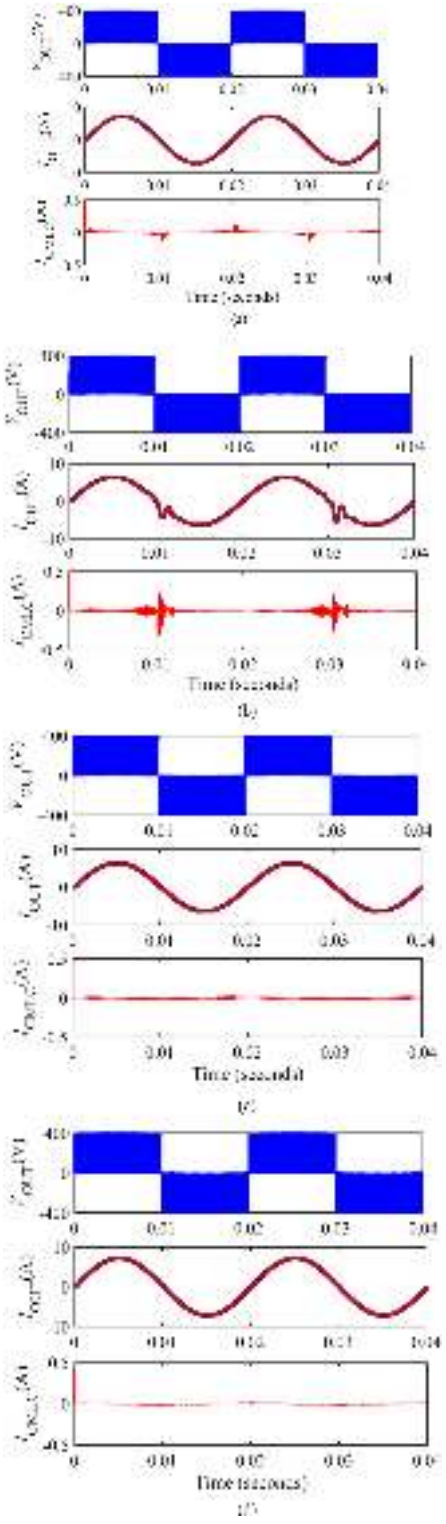


Fig. 4. The Simulation results of V_{out} (upper), i_{out} (central) and i_{leak} (lower) for (**a**) HERIC, (**b**) HBZVR, (**c**) HBZVR-D, (**d**) PN-NPC (**e**) HBZVSCR, (**f**) H6-I and (**g**) proposed H6-D TL-PVI topologies.

Loss studies breakdown and its comparisons

This study demonstrates the loss distributions of different non-NPC and NPC topologies configured at 1 kW rated power using the thermal module in the PSIM software. And detailed simulation device parameters are listed in Table 3[38]. In general losses are categorized into three ways referred as conduction, switching and freewheeling losses[16]. All theoretical calculations are little bit hard to understand but for the reader's understanding here in-detailed loss calculations approach between IGBT and MOSFET based topologies are discussed in here.

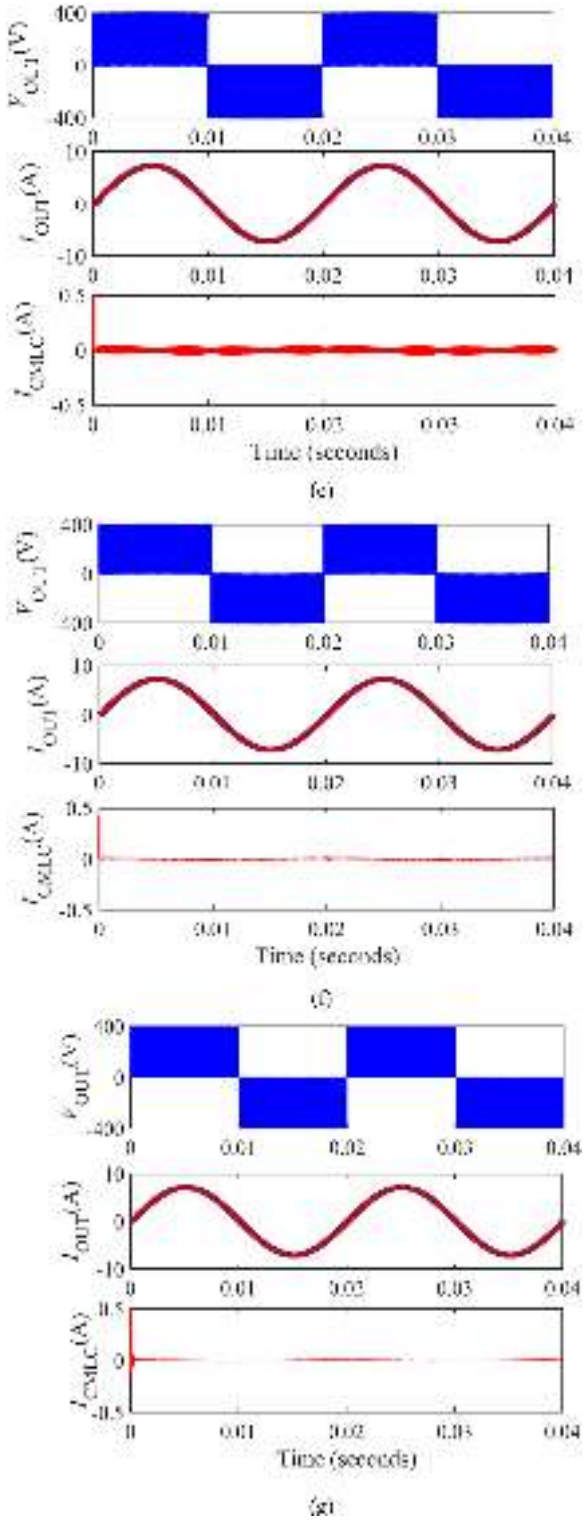


Figure 4. (continued)

For IGBTs conductions, diode and switching losses are calculated by the following Eqs. (10)–(14)[17].

$$P_{Conduction} = V_{CE(SAT)} I_C \tag{9}$$

$$P_{Conduction} = V_F I_F \tag{10}$$

$$P_{SW} = P_{SW-ON} + P_{SW-OFF} \tag{11}$$

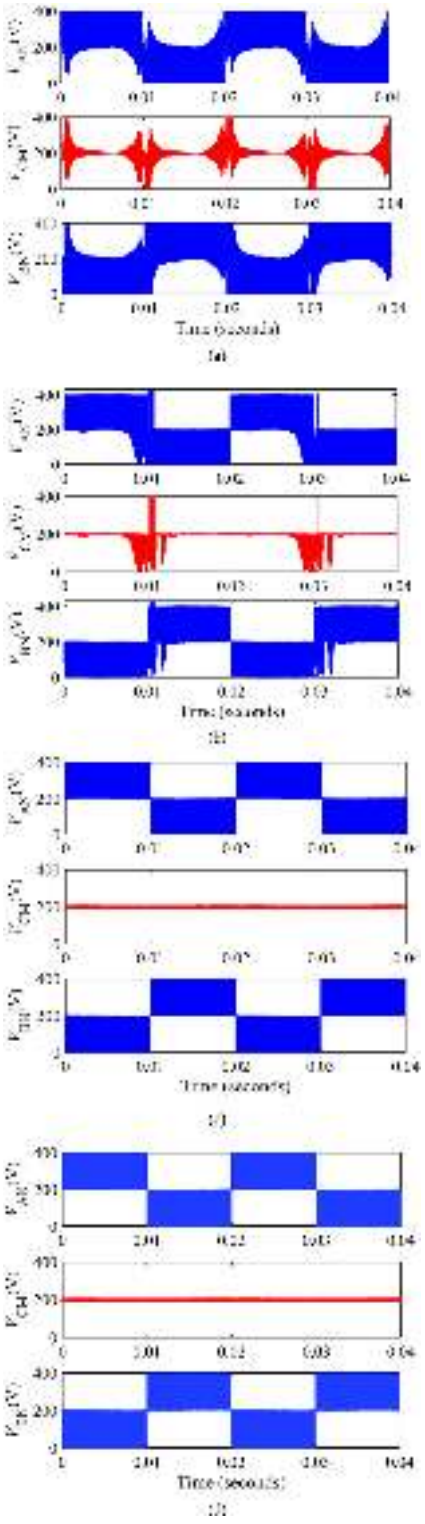
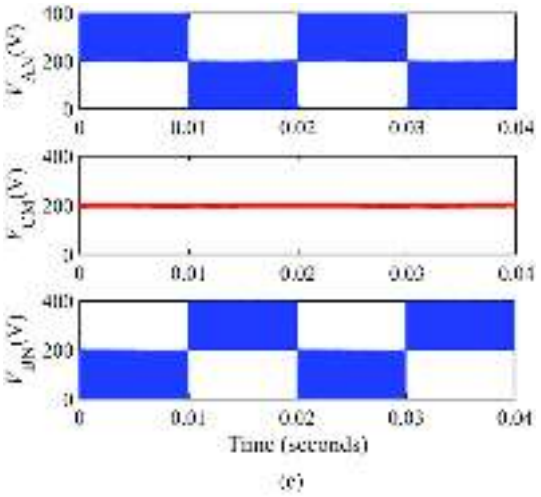
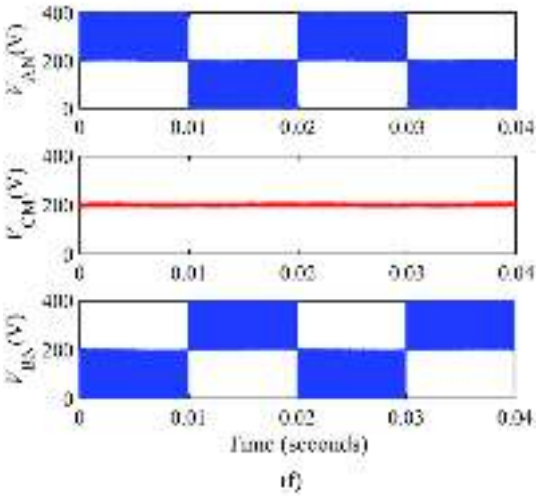


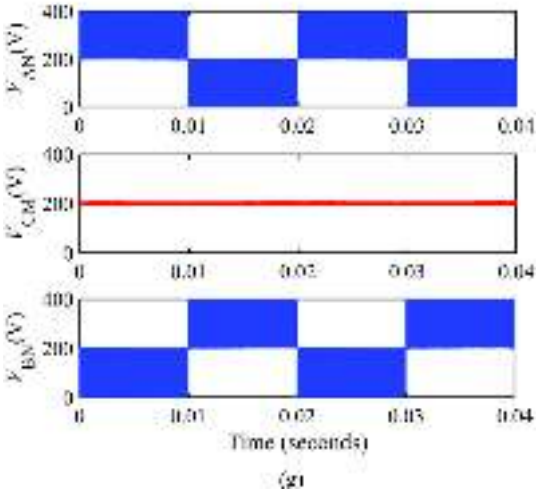
Fig. 5. The Simulation results of V_{AN}, $V_{CM}$and $V_{BN}$for (**a**) HERIC, (**b**) HBZVR, (**c**) HBZVR-D, (**d**) PN-NPC , (**e**) HBZVSCR, (**f**) H6-I and (**g**) proposed H6-D TL-PVI topologies.



(e)



(f)



(g)

Figure 5. (continued)

$$P_{SW-ON} = \frac{E_{on} f V_{dc}}{V_{dc-datasheet}} \tag{12}$$

$$P_{SW-OFF} = \frac{E_{off} f V_{dc}}{V_{dc-datasheet}} \tag{13}$$

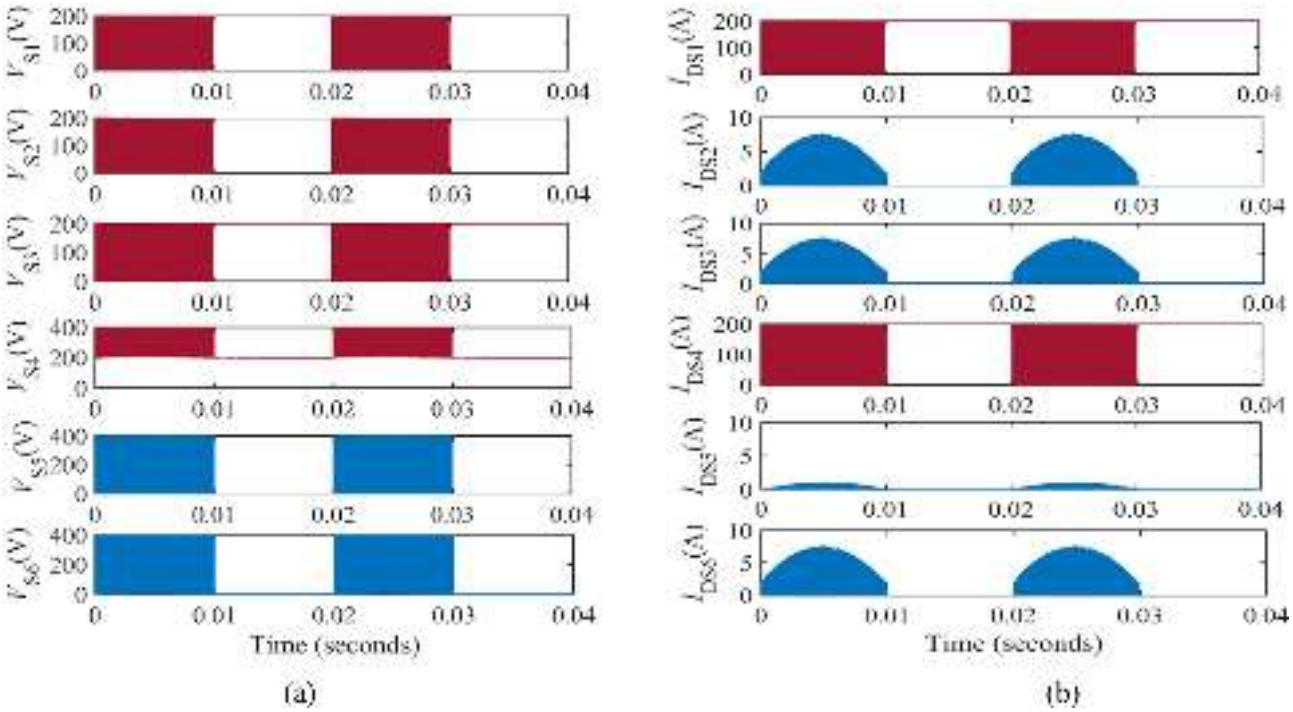


Fig. 6. Proposed H6-D topology stress analysis (**a**) Voltage stress, (**b**) MOSFET body diode drain-source current.

Overall performance	V_{out}	I_{out}	V_{AN}	V_{BN}	CMV	CM-LC
HERIC	Unipolar (+400V,0,−400V)	Sinusoidal	Oscillations(~220V)	Oscillations	Floating(~200V)	<0.3A
HBZVR	Unipolar	Sinusoidal	Oscillations (~230V)	Oscillations	Floating(~200V)	<0.3A
HBZVR-D	Unipolar	Sinusoidal	No Oscillations	No Oscillations	Constant(200V)	<0.03A
PN-NPC	Unipolar	Sinusoidal	No Oscillations	No Oscillations	Constant(200V)	<0.03A
HBZVSCR	Unipolar	Sinusoidal	No Oscillations	No Oscillations	Constant(200V)	<0.03A
H6-I	Unipolar	Sinusoidal	No Oscillations	No Oscillations	Constant(200V)	<0.03A
H6-D	Unipolar	Sinusoidal	No Oscillations	No Oscillations	Constant(200V)	<0.03A

Table 2. Summary and comparison of discussed topologies among proposed H6-D topology.

Parameters		Value
IGBT (600 V)		HGTG20N60A4D
IGBT (1200 V)		FGA15N120
MOSFET (600 V)		SPN04N60C3
MOSFET (1200 V)		ST3030KL
SiC diode		IDD08SG60C
Frequency		50 Hz
Junction Maximum temperature, $T_{j(max)}$		150 °C
calibration factor	P_{cond_Q}	1
	P_{sw_Q}	1
	P_{cond_D}	1
	P_{sw_D}	1

Table 3. Simulation parameter for loss breakdown.

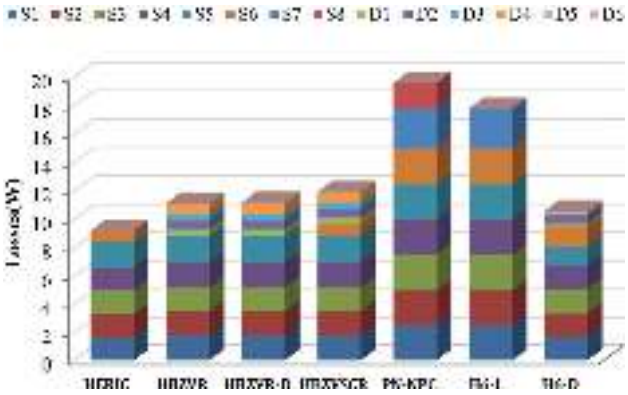


Fig. 7. Device losses.

TL-Inverter		Losses (W)														Total losses (W)
		Conduction losses								Freewheeling diode losses						T_L
		S1	S2	S3	S4	S5	S6	S7	S8	D1	D2	D3	D4	D5	D6	
Non-NPC	H-HERIC	1.6	1.7	1.7	1.6	1.8	0.8	0	0	0	0	0	0	0	0	9.1
	HB ZVR	1.6	1.7	1.7	1.8	1.9	0	0	0	0.4	0.6	0.5	0.7	0.04	0	11.4
NPC	HB ZVR-D	1.8	1.7	1.7	1.8	1.9	0	0	0	0.4	0.6	0.5	0.7	0.04	0.06	11.5
	HBZ VSCR	1.8	1.7	1.7	1.8	1.9	0.8	0	0	0.4	0.6	0.5	0.7	0.04	0	12.3
	PN-NPC	2.5	2.5	2.5	2.5	2.5	2.5	2.5	1.8	0	0	0	0	0	0	19.9
	H6-I	2.5	2.5	2.5	2.5	2.5	2.5	2.5	0	0	0	0	0	0	0	18.1
	H6-D	1.7	1.7	1.7	1.7	1.3	1.1	0	0	0.2	0.6	0.08	0.09	0.05	0.06	10.7

Table 4. Device losses for non-NPC and NPC topologies.

where on-state current is I_C, V_F is forward voltage drop, I_F defines freewheeling current and last $V_{dc-datasheet}$ is actual dc-bus voltage respectively.

And MOSFET losses are calculated by Eqs. (15) and (16)

$$P_{Conduction} = \frac{I_m^2 R_{ds} 2M}{3\pi} \tag{14}$$

$$P_{switching} = f_{sw} E_{oss} \tag{15}$$

where R_{ds} defines the on-state drain-source resistance, I_m is peak output current, M for modulation index, f_{sw} is switching frequency and E_{oss} is energy loss from the device data sheet respectively.

The overall device losses for each inverter are presented in the histogram in Fig. 7, where S1-S7 and D1-D6 represent the active switches and diodes of the discussed inverter topologies, as summarized in Table 4. However, the power loss calculations depend on the accuracy of the device data sheet, which is provided by the manufacturer. For the readers understanding, a comparative loss analysis between IGBT vs. MOSFET losses for heric, and proposed H6-D topologies are highlighted and recorded in Table 5. Therefore, it is noted that MOSFET based topologies are lower losses such as half of the losses are reduced if MOSFET as main power devices than IGBT topologies. However, the theoretical losses are lower than the simulation results because all values are running at real time environment and forward voltage of the device diode. But theoretical values are closer to the simulation results. For the confirmation here conduction, switching and freewheeling loss are included at one place.

Figure 8 highlights the significance of loss distribution using MOSFET designs and seen that the anti-parallel-body diode losses are entirely disregarded. As a result, the overall losses are reduced and this is reason why proposed topology placed in the second lowest losses among the Heric topology. This comprehensive analysis underscores the efficiency and effectiveness of the H6-D design in reducing overall device losses while

Parameter	Value	
MOSFET	SPN04N60C2	
V_{in}	600 V	
V_{ou}	540 V	
T_J	25 °C, 100 °C,150 °C	
R_{ds}	0.8 Ω	
f_{s1}	10 kHz,	
M	0.95	
COSϕ	COSϕ= 0.994	
I_m	0.8–4 A	
Drain source resistance at ON stage	V_{GS}	10 V
	I_D	0.65 A
	T_J	25 °C
	$R_{DS(ON)}$	0.95
E_{oss} cool MOSFET at 400 V	28µJ&46µJ	

Table 5. Thermal device operating conditions.

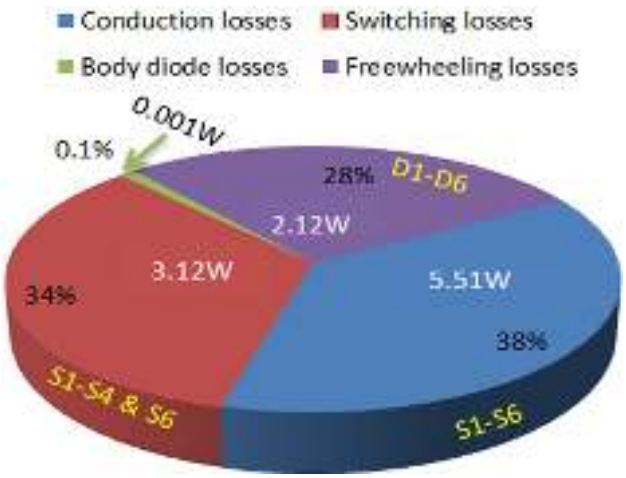


Fig. 8. Proposed topology calculated Loss breakdown.

maintaining high performance efficiency. By effectively minimizing losses, the H6-D design demonstrates a significant improvement over other topologies, making it a highly efficient solution. In addition, the detailed device operation of the discussed non-NPC and NPC topologies to compare their performance against the H6-D topology is outlined in Table 6.

As expected, the non-NPC HERIC TL-PVI topology exhibits the fewer amounts of losses due to the reduced switching count, only with active two MOSFETs during modes 1 and 3, while the other two switches operate at grid frequency during freewheeling periods (modes 2 and 4). Conversely, the HBZVR, HBZVR-D, HBZVSCR, PN-NPC and H6-1 topologies experience the highest device losses due to excessive switching count throughout the grid cycle. Among these, the H6-1 inverter has relatively lower device losses compared to the PN-NPC topology. The H6-D topology, in comparison to the PN-NPC, demonstrates lower losses primarily because it employs MOSFETs as the main power devices, which are only four switches, operate at a lower voltage rating (600 V) and one switch (S5) runs at grid frequency throughout the grid cycle. A key advantage of this setup is that the MOSFETs body diodes do not conduct during operation. This characteristic mitigates the slow reverse recovery time, which otherwise could impose a shoot-through issue on upper and lower complementary devices. Overall, these design choices in the H6-D topology contribute to its enhanced efficiency and reduced losses, making it a more effective solution for transformer-less photovoltaic inverter systems. The other detailed familiar works on loss calculation procedure and theoretical studies have been discussed in[16–18].

Experimental results

Here a practical setup with rating of 1 kW was realized to prove with the simulation results in our laboratory test bench presented in Fig. 9. Table 7listed the specifications of the prototype bed[13]. All control algorithms were developed using the FPGA SPARTAN-6 platform. In this setup, only resistive loads are considered instead of a grid connection for practical development.

Parameters			Non-NPC		NPC				
			HERIC	HB ZVR	HB ZVR-D	HB ZVSCR	PN-NPC	H6-1	H6-D
Total power devices	IGBT		2	0	0	0	4	3	0
	MOSFET		4	5	5	5	4	4	6
	Diodes		0	5	6	5	0	0	6
Voltage stress	V_{dc}		4	4	4	4	2	4	2
	$0.5V_{dc}$		2	1	1	2	6	3	4
Current stress	I_{dc}		4	4	4	4	2	4	2
	$0.5I_{dc}$		2	1	1	2	6	3	4
Conduction loss	$V_g>0$	IGBT	0	0	0	0	2	3	0
		MOSFET	2	2	2	2	2	0	2
	$V_g<0$	IGBT	0	0	0	0	0	3	0
		MOSFET	2	2	2	2	2	0	3
Switching loss	IGBT		0	0	0	0	2	0	0
	MOSFET		2	2	2	2	2	4	2
Freewheeling loss	IGBT		1	0	0	0	2	1	0
	MOSFET		0	1	1	2	0	0	1
	DIODES		1	3	3	2	1	1	3
IGBTs	600 V		2	0	0	0	2	0	0
	1200 V		0	0	0	0	2	3	0
MOSFETs	600 V		4	1	1	4	4	4	4
	1200 V		0	4	5	5	0	0	2

Table 6. Analysis of power device operation.

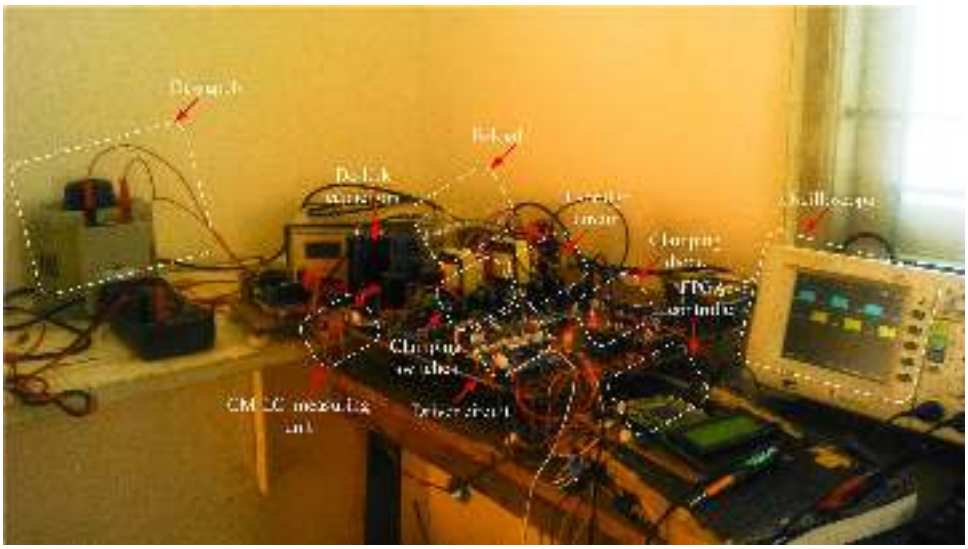


Fig. 9. Experimental set up.

This type of arrangement does not affect the overall performance of the system, as similar assumptions have been made in many topologies, as referenced in[12].

The output response in terms of V_{out} and I_{out} is depicted in Fig. 10. As expected, both non-NPC and NPC topologies generate unique output voltage and current waveforms, such as unipolar and sinusoidal load waveforms. The total harmonic distortion (%THD) of the output load current was measured using the HIOKI 3197 power quality analyzer. The THD values were found to be 2.2%, 1.90%, 1.80%, 1.60%, 1.62%, and 1.43% with respect to the output voltage (V), output current (A), and output power (W) at selected measuring input parameters, as shown in Fig. 10. In Fig. 9(b) and (c), the absence of spikes in the unipolar output voltage indicates no dead time issues, resulting in slightly lower %THD compared to other topologies[39]. Additionally, the proposed new H6-D topology exhibits lower current harmonics compared to other established topologies, mainly because the absence of body-diodes prevents currents from circulating through the anti-parallel body

Parameter		Value
Dc input source voltage		400 V
Maximum power		1000 W
Switching frequency		10 kHz
DC-link capacitor (C_{DC1}, C_{DC2})		1mF,800 V
IGBT	600 V	HGTG20N60A4D
	1200	FGA15N120
MOSFET	600 V	SPAN04N60C3
	1200 V	ST3030KL
SiC diodes		IDD08SG60C
Symmetrical filter L_1, L_2 Inductors		3mH
Capacitive filter-C_f		4μf
Stray capacitor-C_{PV1}, C_{PV2}		100nF
Resistive load		50Ω
Controller		FPGA SPARTAN-6

Table 7. Prototype specifications.

diode of the MOSFET switches. This absence of body-diodes explains why the THD is lower in the proposed topology.

Figure 11 illustrates the common mode analysis of both non-NPC and NPC topologies. The common mode leakage current magnitudes for the Heric, HBZVR, HBZVSCR, PN-NPC, H6-I, and H6-D topologies are 29.19 mA, 27.13 mA, 13.94 mA, 13.46 mA, 13.43 mA, and 12.84 mA, respectively. It is observed that all configurations comply with VDE-AR-N 4105 and VDE0126-1-1 standards, with the proposed H6-D topology exhibiting the lowest common mode leakage current. Non-NPC topologies have double the common mode leakage current compared to NPC topologies due to poorer clamping ability during the freewheeling period, as explained earlier.

As expected, the non-NPC Heric and HBZVR topologies exhibit oscillating V_{AN}, V_{CM}, and V_{BN} voltages with spikes up to 220 V, significantly increasing common mode leakage current, as seen in Fig. 12(a) and (b). This confirms that using PWM methods alone fails to generate a constant common mode voltage (CMV). Therefore, the realization of clamping circuits in NPC-based HBZVSCR, PN-NPC, H6-I, and H6-D topologies achieves constant CMV practically, clarifying why common mode leakage current is considerably suppressed, as seen in Fig. 12(c-f).

Figure 13 illustrations the voltage stress on S1, S2 and S3, S4 switches, which are good agreement with theoretical device operation in Table 7 such as exactly clamped at 200 V for the given input dc voltage.

The European efficiency is computed based on the following equation given below (16)[28].

$$\eta_{EU} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \quad (16)$$

Efficiency measurements were conducted using the HIOKI 3197 power analyzer. The calculated efficiency performance analysis of both non-NPC and NPC inverters is illustrated in Fig. 14, showing efficiencies of 98.13%, 94.28%, 95.10%, 96.42%, 96.18%, and 97.25% for the Heric, HBZVR, HBZVSCR, PN-NPC, H6-I, and H6-D topologies, respectively. The proposed H6-D TL-PVI topology achieved the second-highest efficiency, surpassed only by the Heric topology. This high efficiency is attributed to the low switching count during freewheeling modes and the presence of only one grid frequency switch.

Overall performance comparisons are summarized in Table 8. These results demonstrate that the H6-D topology not only reduces common mode leakage current (CM-LC) and total harmonic distortion (%THD) but also offers high efficiency, making it a superior choice for transformer-less photovoltaic inverter systems.

Conclusion

This article reviews various single-phase, highly efficient, and low common-mode leakage current (CM-LC) transformerless PV inverter topologies from the H6 family, including both non-neutral point clamped (non-NPC) and neutral point clamped (NPC) configurations. The analysis reveals that non-NPC topologies, such as Heric and HBZVR, achieve excellent efficiency but demonstrate poor common-mode (CM) performance. In contrast, NPC topologies like HBZVSCR, PN-NPC, and H6-1 excel in reducing CM-LC but incur higher losses. To address these trades-offs, a novel neutral-point-clamped H6 MOSFET inverter, referred to as H6-D, is proposed. This new topology combines the low-loss characteristics of non-NPC methods with the CM-LC reduction capabilities of NPC methods. The performance of the H6-D topology is evaluated and compared to established non-NPC and NPC topologies across key metrics, including common-mode voltage (CMV), common-mode leakage current (CM-LC), losses, total harmonic distortion (%THD), voltage stress, and

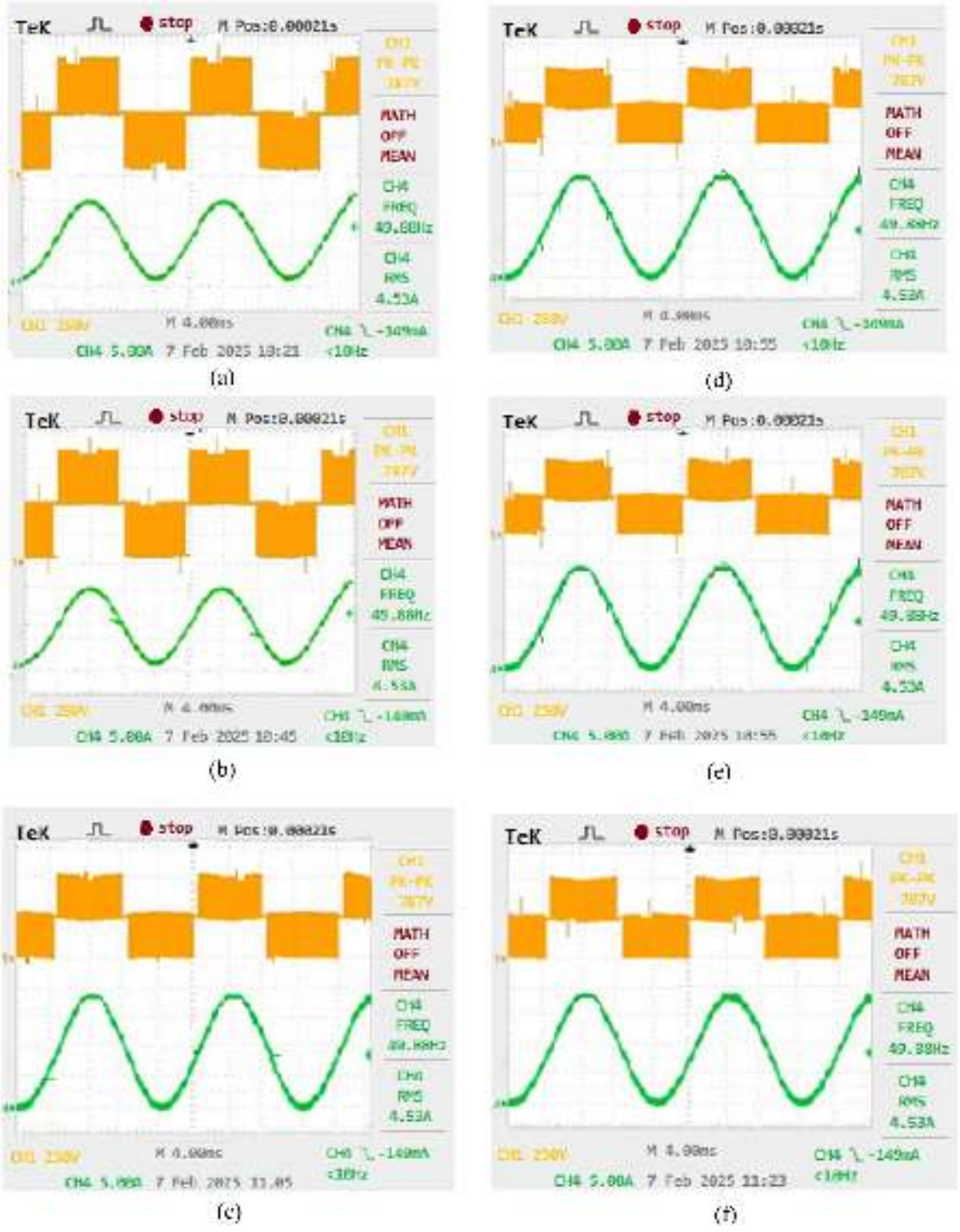


Fig. 10. Experimental test results of differential mode output voltage (V_{AB}) and output load current (i_{out}) for (**a**) Heric, (**b**) HBZVR, (**c**) HBZVSCR, (**d**) PN-NPC, (**e**) H6-I and (**f**) proposed H6-D TL-PVI topologies.

efficiency. Experimental results demonstrate that the H6-D topology delivers superior performance across all parameters, making it an ideal solution for high-efficiency photovoltaic (PV) applications.

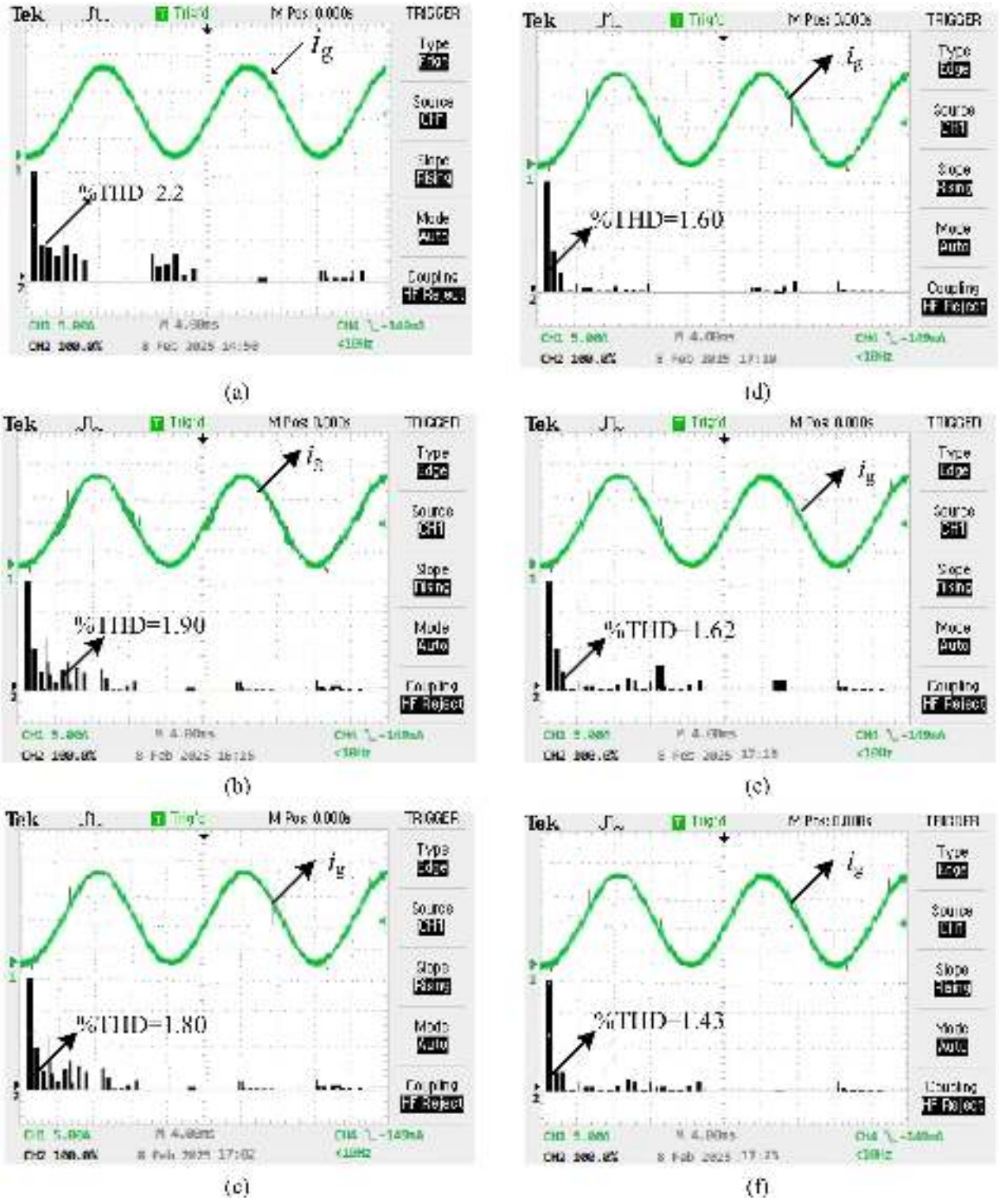


Fig. 11. Total harmonic Distortion (**a**) Heric, (**b**) HBZVR, (**c**) HBZVSCR, (**d**) PN-NPC, (**e**) H6-1, (**f**) H6-D.

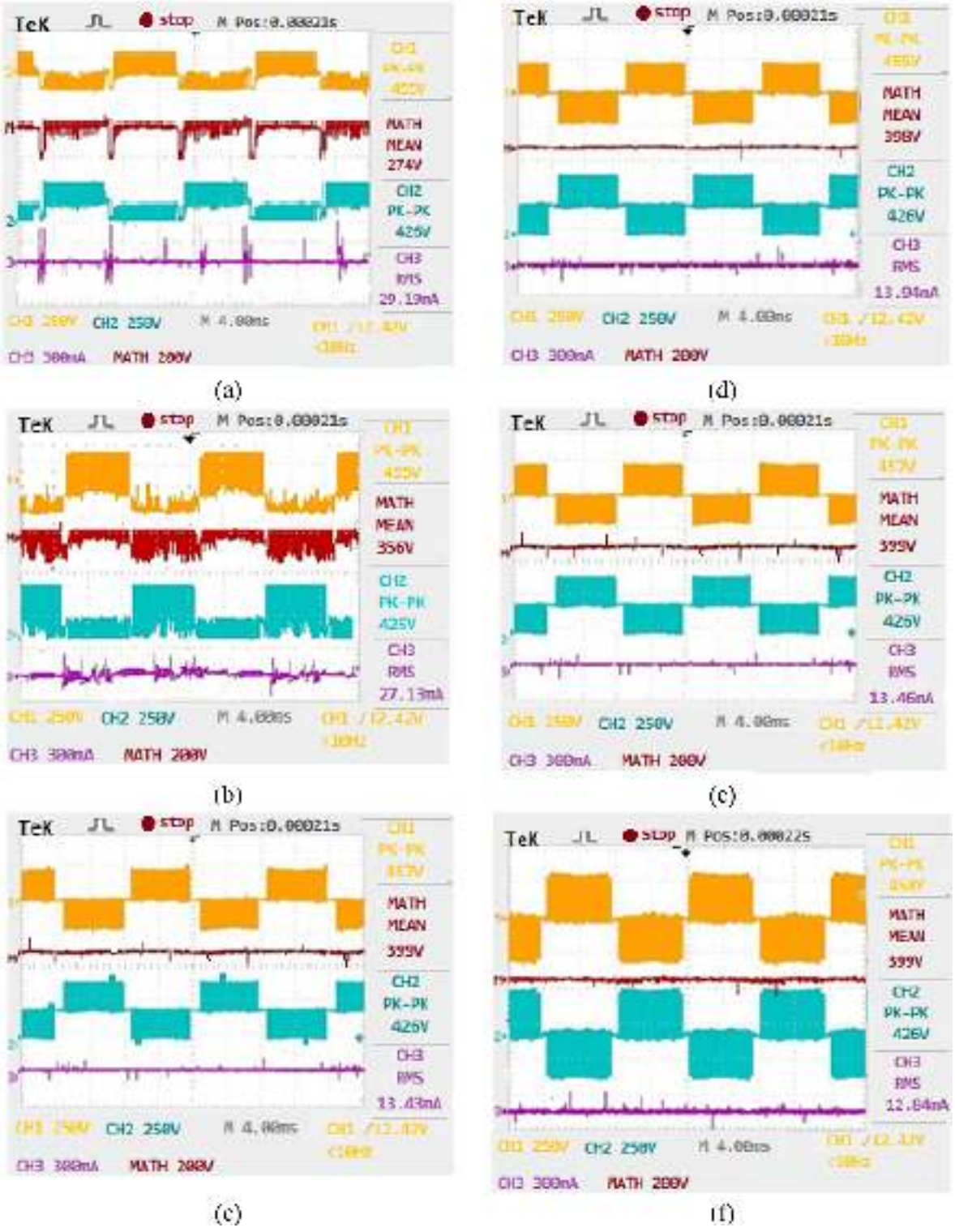


Fig. 12. Experimental results of V_{AN}, $2V_{cm}$, V_{BN}, and CM-LC (i_{leak}) for (**a**) Heric, (**b**) HBZVR, (**c**) HBZVSCR, (**d**) PN-NPC, (**e**) H6-I and (**f**) proposed H6-D TL-PVI topologies.

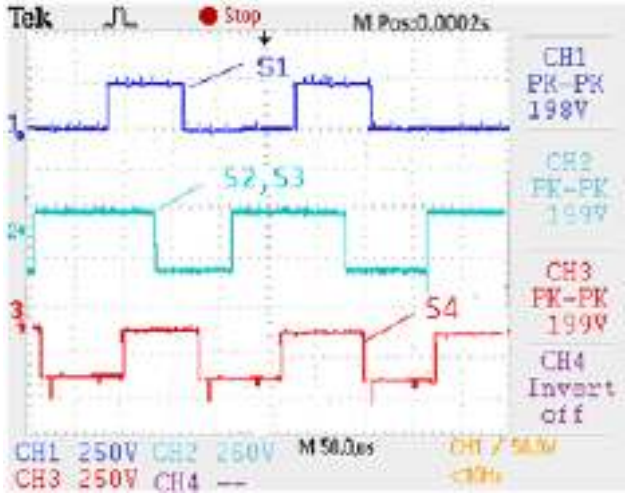


Fig. 13. Voltage stress across S1, S2 and S3, S4.

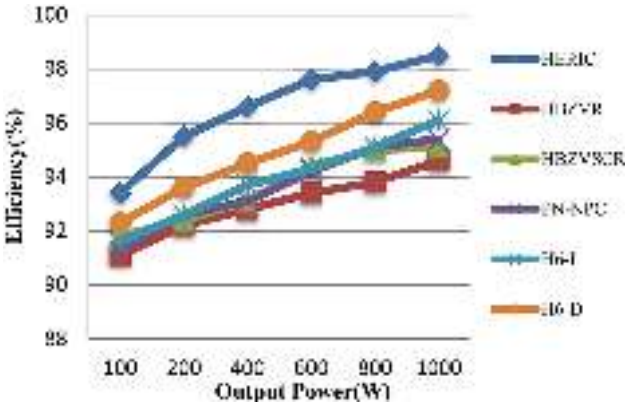


Fig. 14. Efficiency analysis.

Topology	Non-NPC		NPC			
	HERIC	HBZVR	HBZVSCR	PN-NPC	H6-I	H6-D
PWM	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
CMV	Floating (~ 200 V)	Floating (~ 200 V)	Constant (200 V)	Constant (200 V)	Constant (200 V)	Constant(200 V)
CM-LC (mA_{rms})	29.19	27.13	13.94	13.46	13.43	12.84
THD_i (%)	2.2	1.90	1.80	1.60	1.62	1.43
Voltage stress	Low ($0.5V_{dc}$)	High (V_{dc})	High (V_{dc})	High (V_{dc})	high(V_{dc})	Low ($0.5V_{dc}$)
European efficiency (%)	98.13	94.28	95.10	96.42	96.18	97.25
Maximum efficiency (%)	98.56	94.56	95.26	96.86	97.29	97.90

Table 8. Performance comparison among Non-NPC and NPC Tl-PVI topologies.

Data availability

The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

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Author contributions

Author Contributions: Data curation, A.S.; Formal analysis, A.S., and S.B.T; Funding acquisition, S.B.T. and

M.K.; Methodology, A.S., and X.G.; Project administration, S.B.T. and M.K., Resources, A.S.,, and X.G.; Supervision, X.G.; Writing–original draft, A.S. and X.G. All authors have read and agreed to the published version of the manuscript.

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Declarations

Competing interests
The authors declare no competing interests.

Additional information
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