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A FinFET-based static memory cell optimized for stability and low power consumption

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Abstract

As the semiconductor industry continues to push the boundaries of miniaturization, traditional MOSFET transistors are no longer the ideal choice for VLSI circuit design, particularly for memory cells where stability and power efficiency are critical. FinFET transistors, with their superior performance in mitigating process variations, enhancing gate control, and reducing leakage currents, offer a promising alternative. This paper presents a novel 9 T SRAM cell, carefully designed and simulated using 10 nm FinFET devices at a supply voltage of 0.55 V. The proposed cell achieves significant improvements in read stability (writability) through the implementation of read path isolation and feedback-cutting techniques, resulting in a minimum enhancement of 1.10 (1.19) times. Furthermore, the cell significantly reduces read, write, and leakage power by at least 7.03%, 8.66%, and 14.14%, respectively. These power reductions are attributed to the adoption of a single-bitline structure, transistor stacking in access paths, and the minimization of control signal activation. To ensure robust operation in real-world scenarios, the cell's resilience to process variation is meticulously examined. Analysis reveals lower variability in both read stability and writability design metrics, demonstrating the cell's inherent robustness to manufacturing imperfections.

1. Introduction

Static random access memories (SRAM) are utilized as cache memories in microprocessors, occupying a significant portion of the chip area due to their repetitive structures and high logical performance [1–4]. Therefore, reducing the power consumption of SRAMs can significantly decrease the overall power consumption. The supply voltage has a substantial impact on the total power consumption because decreasing the supply voltage (V_{DD}) leads to a reduction in dynamic power and leakage power in a linear and quadratic manner, respectively [3, 5, 6]. However, lowering V_{DD} results in increased operational delay, causing an increase in energy consumption per read and write cycle [7–10]. Additionally, at lower voltages, the noise margin decreases due to the reduced voltage difference between V_{DD} and the threshold voltage, making the circuit less reliable [11–13]. Thus, designing a low-power SRAM cell with improved stability poses a significant challenge. It is also important not to overlook the reduction in occupied space by SRAM cells. To maximize density and minimize occupancy, SRAM cells should utilize transistors with the smallest size in each technology [7, 14]. However, reducing the size of transistors in nanometer dimensions affects the efficiency of SRAM cells, leading to issues such as increased leakage current and short-channel effects [15–19]. Fin-based field-effect transistors (FinFET), with features such as low leakage power, low threshold voltage, high drive current, better gate control, and suppression of short-channel effects, offer a promising technology that can replace metal-oxide-semiconductor FETs (MOSFET) and aid in scaling down transistor dimensions to less than 22 nanometers [20–22].

Despite the advantages FinFET technology offers for memory cell design, the common 6 T cell does not exhibit desirable stability at low supply voltages due to the transistor sizing requirements. This instability undermines the reliability of the cell [20]. Another challenge with the basic cell is the half-select problem, as it uses a single control line for both reading and writing operations, potentially allowing non-selected bitlines in the row to alter data stored in those cells during a write operation [23, 24]. Therefore, restructuring the 6 T cell and redesigning it using new low-power transistors like FinFETs is necessary. Achieving a low-power, stable, and parametrically robust SRAM cell requires improvements at both the design and device levels.

One of the key parameters affecting power consumption in SRAM cells is the bitlines because they have long wiring, capacitive load, and high activity. Therefore, reducing the number of bitlines can be a method to reduce power consumption [25]. However, this does not always mean improved circuit performance because it can lead to a decrease in noise margin and cell stability. For this reason, cells have different bitline configurations based on their purpose and cell layout [26].

The conventional 6 T SRAM cell, despite its simple and compact structure using two bitlines for both read and write operations, works with higher power and reduced noise margin [27]. In [28], a nine-transistor SRAM cell is presented, which improves read static noise margin (RSNM) using a separate read path and enhances write static noise margin (WSNM) using a feedback-cut technique. This cell utilizes two bitlines, one for reading and the other for writing. In cells [7, 24, 29], only one bitline is used for both read and write operations to reduce dynamic power consumption. In cells [24] and [29], the RSNM has improved due to the consideration of a separate read path. However, the cell [7] suffers in reading due to the lack of isolation of the read paths from the storage nodes, leading to lower static read margins. Near the threshold voltage, many SRAM cells fail to guarantee a minimum write capability of six-sigma (6σ), hence writing assist techniques are used. However, these techniques depend on the chosen assist method and can compromise the retention stability in semi-selected cells, resulting in increased energy consumption [27].

Power-gating write assist is employed in the cells of [30–32], while in the cells of [24, 25, 28], and [29], a feedback-cut assist writing technique is used, leading to high noise write margins for all these cells. However, the cells in [29] and [30] provide lower WSNM compared to other cells due to the use of two series transistors in their writing path. These cells [29] and [30] are half-select-disturb free owing to using row- and column-based control signals (cross-point write wordlines selection) and can support the bit-interleaving architecture.

The half-select-disturb issue in the cells such as [20, 33, 34], and [35] has also been resolved. Another important parameter in SRAM cell design is the read and write access time, which depends on the number and arrangement of transistors in the read and write paths in the cell. The 6 T cell has a differential writing structure, hence it offers less delay compared to single-ended cells [20]. The cells such as [7, 20, 24, 28–30, 33], and [34] have a single-ended structure, among which cells with high internal capacitance and long access paths provide higher delays compared to other cells.

To overcome the challenges associated with SRAMs, a nine-transistor SRAM cell based on 10 nm FinFET technology with high stability and low power consumption is proposed in this paper. The proposed cell uses one bitline for both read and write operations to reduce dynamic and static power consumption. It also implements a separate read path isolation technique to enhance RSNM and a feedback cut mechanism to improve WSNM. Furthermore, by using series transistors in the access path and placing the WE signal in the logical '0' state to prevent leakage in the read path, the proposed cell offers low leakage power. It is noteworthy that by addressing half-select-disturb issue, the proposed cell can also support a bit interleaving structure.

2. Proposed 9T SRAM design

The schematic diagram of the proposed single-ended nine-transistor SRAM cell is shown in figure 1(a). The core of this cell uses two n-type transistors (N1, N2) and three p-type transistors (P1, P2, P3) to store and complement data in storage nodes Q and QB. The p-type transistor (P3) is controlled by the WWL signal and is connected to the input of the right inverter (Q2) and the output of the left inverter (Q). This transistor is responsible for breaking the feedback path during the write operation, leading to facilitating the write operation and hence improving WSNM. Transmission gate (TG) formed by N4 and P5 transistors, along with n-type transistor (N3) are used to access the bitline to the storage nodes, controlled respectively by WL and its complement ($\overline{\text{WL}}$) and WWL. In the proposed structure, the read path is separated from the storage nodes using the TG and transistor P4 powered by signal WE, through the use of n-type transistor (N3), resulting in a significant improvement in RSNM. Figure 1(b) depicts the sequence read/write operation in the proposed design to ensure that it works properly. The status of the control signals used in the proposed cell during the different operations is given in table 1.

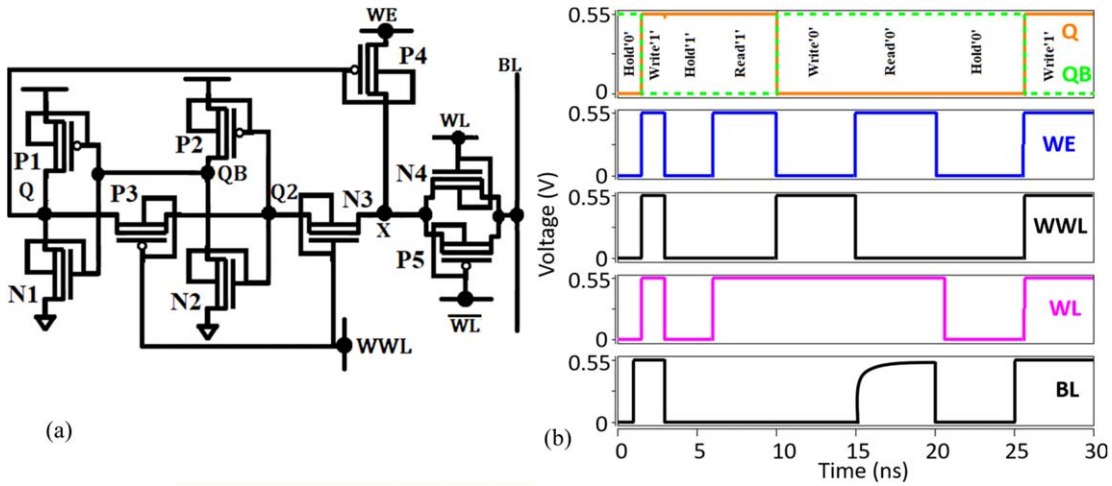

Figure 1. Proposed 9 T SRAM cell. (a) Cell schematic and (b) Transient resposne.

Table 1. Proposed 9 T SRAM cell's control signal status.

Signal	Hold	Read	Write '0'	Write '1'
BL	'0'	'0'	'0'	'1'
WL	'0'	'1'	'1'	'1'
WWL	'0'	'0'	'1'	'1'
WE	'0'	'1'	'0'	'1'

2.1. Hold operation

During the retention operation, WL signal is set to logical '0', deactivating the TG (P5 and N4). The signal WWL is also set low to activate feedback path. In this state, there is no path for accessing the bitline to the storage nodes. Additionally, in the read path, the WE signal is set to '0', turning off the power supply of transistor P4. Cutting off the power supply helps to reduce leakage in the proposed cell's read path to the bitline BL.

In the hold mode, the SRAM cell is power-consuming because it is responsible for holding the stored data most of the times. The power consumed by the SRAM cell in this mode is a type of leakage power (P_L), which can be mathematically expressed by equation (1), where I_{sub} is the subthreshold leakage current, which is the main component of leakage power [32]. By considering that the proposed SRAM cell is holding '1' and '0' at node Q, equation (1) can be rewritten by equations (2) and (3), respectively.

$$P_L = \sum I_{sub} \times V_{DD} \tag{1}$$

$$P_{L-hold1@Q} = V_{DD} \times (I_{sub-N1} + I_{sub-P2} + I_{sub-N3} + I_{sub-P4} + I_{sub-N4} + I_{sub-P5}) \tag{2}$$

$$P_{L-hold0@Q} = V_{DD} \times (I_{sub-P1} + I_{sub-N2}) \tag{3}$$

2.2. Read operation

In the read operation, the control signal WWL is set low to turn off the write access transistor N3, disabling any writing path in the cell. On the other hand, the feedback cut-off transistor P3 is turned on, establishing a feedback path between the complementary inverters. In this mode, WE is pulled up to V_{DD}. Before starting the read operation, bitline BL is precharged to '0'. Then, with WL signal set to logical '1', the TG is activated, initiating the read operation. Suppose node Q has stored a logical '0'. At this point, transistor P4 is turned on, allowing the bitline BL capacitor to be charged through a path consisting of the TG(P5 and N4) and transistor P4. However, if node Q holds a logical '1', transistor P4 is turned off, keeping the bitline BL at '0'.

The read current (I_{read}) is the current flow through the access switch TG from the WE during the read operation. The I_{read} in the proposed 9 T SRAM cell can mathematically be expressed by applying the Kirchoff's current law (KCL) at node X (refer to figure 1). At node X, current comes in through P4 and goes out through TG (two paths—N4 and P5). The I_{read} formula is given by equation (4).

Table 2. 10 nm FinFET technology model file's parameters.

Parameters	n-type FinFET	p-type FinFET
Channel length (nm)	14	14
Fin height (nm)	21	21
Fin thickness (nm)	9	9
Body doping (cm^{-3})	2.5×10^{16}	2.5×10^{16}
Source/Drain doping (cm^{-3})	3×10^{20}	3×10^{20}
Threshold voltage (V)	0.32	−0.32
Gate work function (eV)	4.604	4.565

$$\begin{aligned} I_{read} = \; & I_{P4}(V_{GS} = V_Q - V_{WE},\; V_{DS} = V_X - V_{WE}) \\ = \; & I_{N4}(V_{GS} = V_{WL} - V_{BL},\; V_{DS} = V_X - V_{BL}) \\ & + I_{P5}(V_{GS} = V_{\bar{WL}} - V_{BL},\; V_{DS} = V_X - V_{BL}) \end{aligned} \tag{4}$$

2.3. Write operation

In the write operation of this cell, a cross-coupled feedback method between the inverters is used. This technique involves deactivating transistor P3 during writing, dividing the voltage between the access transistor with the pull-up and pull-down transistors, making the write operation easier with less power and greater noise margin. For writing operations, row-based WL and column-based WWL signals must be activated to access the bitline to the storage nodes. The write operation varies based on the data being written. To achieve write '0' operation, the bitline and WE signal are set to a logical '0'. Then, node Q2 is discharged through a path consisting of the TG and transistor N3. By decreasing the voltage level of node Q2 and reaching the threshold voltage of the right inverter, transistor P2 is turned on, connecting node QB to V_{DD}, charging it. Subsequently, the stored data in node QB is discharged by turning on transistor N1. Writing '1' in the cell is similar to writing '0', except that the bitline BL and WE signal are loaded to '1', and besides the access transistors P5, N4, and N3 being on, transistor P4 is also turned on due to the '0' stored in node Q, enhancing writing '1' in node Q2 using the WE signal. This way, the value '1' is written to node Q2 and ultimately transferred to node Q through two inverters.

The write current (I_{write}) is the current flow through the access switch TG from the BL during the write operation. The I_{write} in the proposed 9 T SRAM cell for writing '1' to '0' storing node Q can mathematically be represented by applying the KCL at node X (see figure 1). At node X, current comes in through P4 and TG (two paths—N4 and P5) and goes out through N3, as given in equation (5).

$$\begin{aligned} I_{write} = I_{P4}(V_{GS} = V_Q - V_{WE},\; V_{DS} = V_X - V_{WE}) + I_{N4}(V_{GS} = V_{WL} - V_{BL},\; V_{DS} = V_X - V_{BL}) \\ + I_{P5}(V_{GS} = V_{\bar{WL}} - V_{BL},\; V_{DS} = V_X - V_{BL}) \\ = I_{N3}(V_{GS} = V_{WWL} - V_X,\quad V_{DS} = V_{Q2} - V_X) \end{aligned} \tag{5}$$

As earlier noted, the BL is grounded during write '0' operation and raised to V_{DD} during write '1' operation in the proposed SRAM design. Then, both the row-based signal WL and column-based signal WWL need to be activated simultaneously to write data to the cell. Since each column is individually selected through the values of the columnar signal WWL, the cell effectively implements a cross-point write mechanism [30]. This inherent design feature inherently eliminates write half-select disturbance, ensuring data integrity during write operations.

3. HSPICE simulation results for SRAM designs

The novel 9 T SRAM cell was designed and simulated using the HSPICE simulator with a 10 nm FinFET technology model (parameters given in table 2) [36, 37]. The performance of this cell, including RSNM, WSNM, read/write delays, and power consumption (read, write, and leakage), was compared to conventional 6 T [38], SB9T [24], ST9T [7], TRD9T [28], and HFWA9T [29] SRAM cells. All the above-mentioned SRAM cells have been redesigned and re-simulated using the 10 nm FinFET technology model, which is available in [36]. Since the convetnional 6 T SRAM cell needs to be sized properly to have correct read and write operations, we have assigned two Fins to the pull-down transistors in the cross-coupled inverters and one fin to the remaining transistors. All SRAM cells under investigation have been sized accordingly for fair comparison [39].

Although lowering V_{DD} leads to a decrease in both dynamic power and leakage power, however, it also increases operational delay. To have a trade-off between delay and power, it is recommended to lower the value of V_{DD} near the transistior's V_{th} [7]. Still, lowering V_{DD} value very close to the V_{th} is not possible because

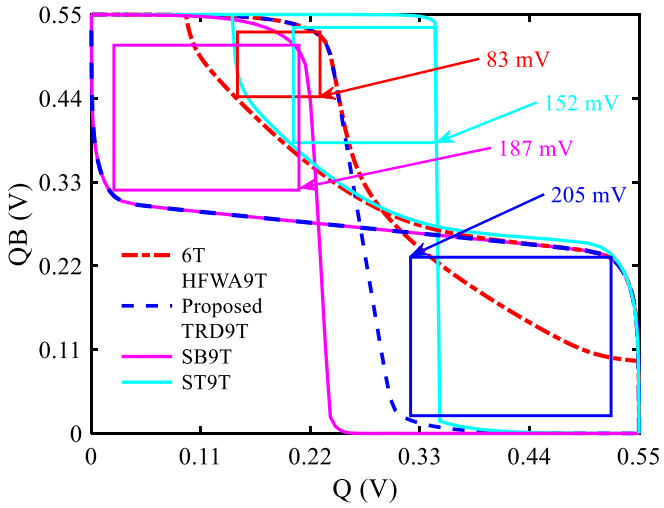

Figure 2. RSNM of investigated SRAM cells at $V_{DD} = 0.55$ V.

conventional 6 T fails to do correct read/write operations. Therefore, the simulations have been conducted at $V_{DD} = 0.55$ V and room temperature (25 °C).

Process variations pose significant challenges in designing nanoscale circuits, particularly for FinFET-based designs. Variations in fin height, fin width, and channel length are primary sources of parametric variability, impacting circuit performance and reliability. Decreasing channel length and increasing silicon thickness exacerbate short-channel effects such as drain-induced barrier lowering and threshold voltage roll-off, leading to increased leakage currents. Fin height plays a crucial role in determining the effective channel width and drive current of the device [40]. Variations in these dimensions can significantly impact power consumption, performance, and the robustness of SRAM cells. To assess the impact of process variations, Monte-Carlo (MC) simulations with 5000 iterations were performed using a Gaussian distribution with ±10% variations at the $\pm 3\sigma$ level [27].

3.1. Read static noise margin

The read static noise margin (RSNM) for an SRAM cell is a crucial parameter that measures its resistance to noise during the read operation. It quantifies the amount of noise voltage that can be tolerated on the bitline before the stored data bit is erroneously read. A larger RSNM ensures that the cell can accurately read data even when subjected to significant noise disturbances. The RSNM is graphically defined as the side length of the largest square that can be inscribed within the smaller 'wing' of the read butterfly curve [11].

Figure 2 illustrates the read butterfly curves for all studied SRAM cells, with the largest inscribed square and corresponding RSNM values highlighted. These curves were extracted at $V_{DD} = 0.55$ V. The 6 T cell exhibits the lowest RSNM due to its susceptibility to read disturbance, as it lacks a dedicated read isolation path. The ST9T cell, incorporating hybrid cross-coupled inverters (conventional and Schmitt-trigger), effectively mitigates read disturbance, resulting in a higher RSNM compared to the 6 T cell. While the SB9T cell employs a read-decoupling technique, the use of stacked p-type transistors in its left inverter reduces the trip point voltage, leading to a lower RSNM. In contrast, the TRD9T, HFWA9T, and the proposed 9T SRAM cells demonstrate significantly enhanced RSNM values: 2.47, 1.35, and 1.10 times higher than the 6 T, ST9T, and SB9T cells, respectively. This improvement is attributed to the complete isolation of their storage nodes from the read bitline.

The RSNM was evaluated for a range of V_{DD} values, starting at 0.55 V and increasing to 0.75 V in steps of 0.1 V. The results are presented in figure 3. As observed, the RSNM value exhibits a direct correlation with V_{DD}, increasing as V_{DD} increases. Notably, the proposed 9 T SRAM cell consistently demonstrates a high RSNM across all simulated V_{DD} values.

3.2. Write static noise margin

The write static noise margin (WSNM) is a key indicator of an SRAM cell's robustness during write operations. It represents the maximum noise voltage that can exist on the bitline without causing an incorrect write to the cell. In essence, a higher WSNM signifies greater resilience to noise during data storage. This translates to a more reliable memory cell, capable of accurately writing data even in the presence of significant noise disturbances.

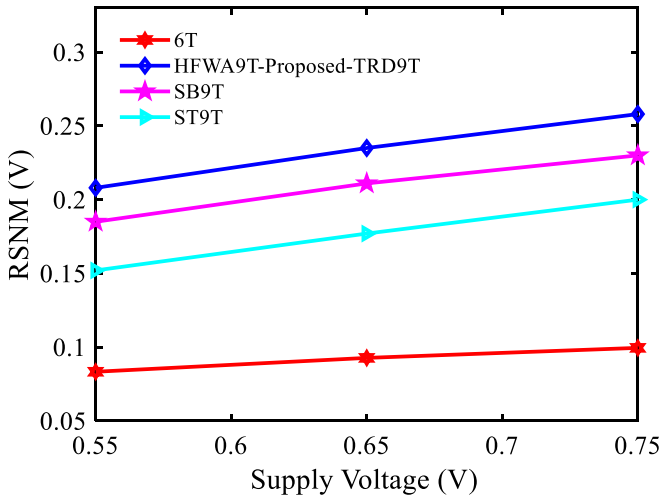

Figure 3. RSNM of investigated SRAM cells versus V_{DD}.

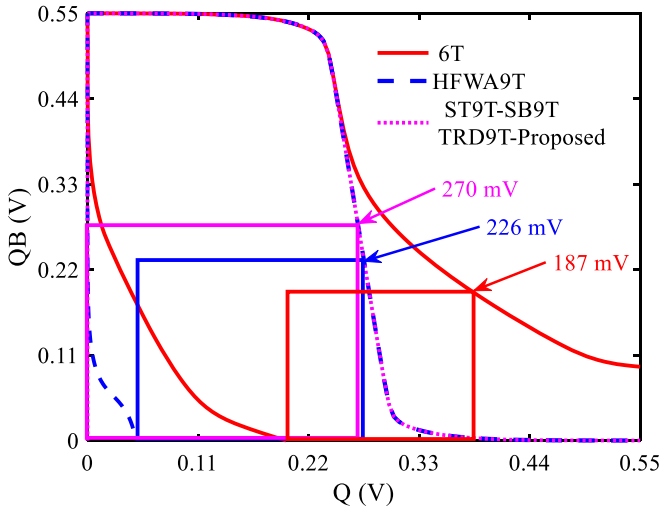

Figure 4. WSNM of investigated SRAM cells at $V_{DD} = 0.55$ V.

The WSNM is graphically represented as the side length of the smallest square that can be inscribed within the lower half portion of the combined inverters' read/write voltage characteristics [32].

Figure 4 illustrates the combined read/write voltage characteristics of the cross-coupled inverters for all studied SRAM cells. The smallest inscribed square and corresponding WSNM values are highlighted, measured at $V_{DD} = 0.55$ V. The 6 T cell exhibits the lowest WSNM due to the absence of a write-assist technique. The other investigated SRAM cells utilize a feedback-cutting technique to enhance WSNM. However, the HFWA9T cell experiences a reduction in WSNM due to the presence of stacked n-type transistors in its write path. The proposed 9T SRAM cell demonstrates significantly improved WSNM, achieving 1.44 and 1.19 times higher values than the 6 T and HFWA9T cells, respectively. Figure 5 explores the impact of V_{DD} variation on WSNM across the different SRAM cells. As V_{DD} increases, WSNM also increases. Notably, the proposed design consistently displays high WSNM across all tested V_{DD} values.

3.3. Read and write delays

Read and write delays are crucial performance metrics for SRAM cells, determining how quickly data can be accessed and stored. They represent the time required for the cell to complete a read or write operation [3].

The measurement approach for read delay differs between differential and single-ended SRAM cells:

- Differential reading SRAM: The read delay is defined as the time taken for a 50 mV difference to develop between the two bitlines after the wordline is activated [29].

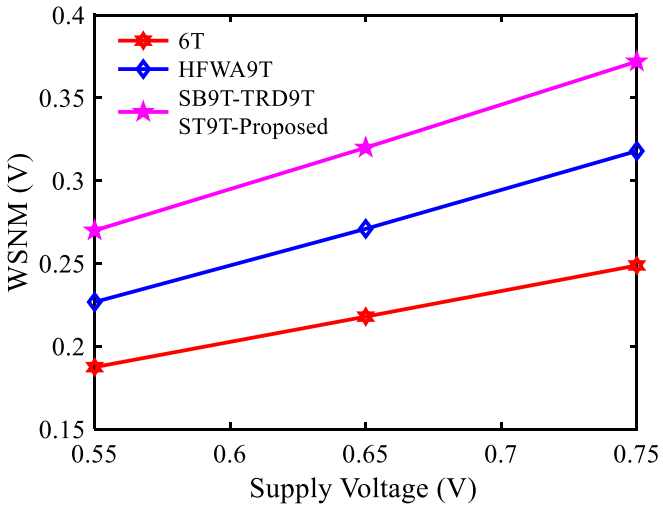

Figure 5. WSNM of investigated SRAM cells versus V_{DD}.

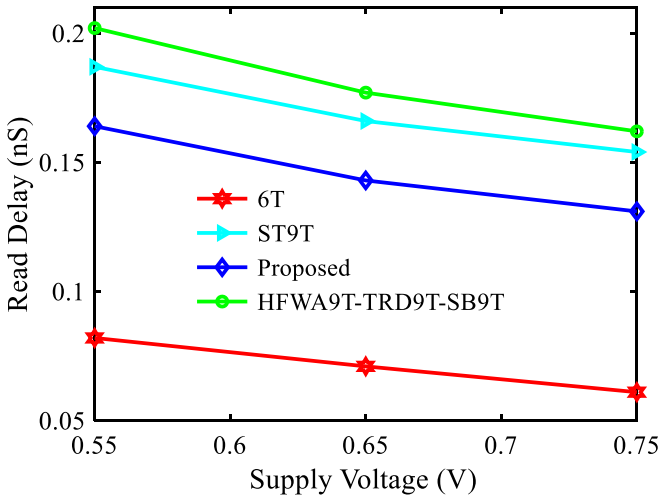

Figure 6. Read delay of investigated SRAM cells versus V_{DD}.

- Single-ended reading SRAM: The read delay is the duration starting from the activation of the wordline for reading until the bitline voltage either drops to 0.8 times the V_{DD} or rises to 0.2 times the V_{DD} [41].

The conventional 6 T SRAM cell, with its fully differential structure, exhibits the lowest read delay among the investigated cells. The SB9T, TRD9T, and HFWA9T cells, due to the inclusion of two stacked n-type transistors in their read path and a grounded control signal, experience a higher read delay. Similarly, the ST9T cell's three-stacked transistors in the read path contribute to a slower read operation compared to the proposed 9T design. The proposed 9T SRAM cell employs a TG in its access path, which significantly speeds up the read operation. This is because the TG creates a low-resistance path between drian and source terminals, allowing logic '0' or '1' to pass through without significant loss. Figure 6 compares the read delays of the investigated SRAM cells at various V_{DD} values. While the proposed 9T cell shows a 2 times higher read delay compared to the 6 T cell at $V_{DD} = 0.55$ V, it outperforms the ST9T and SB9T cells by 12.30% and 18.81%, respectively, demonstrating its improved read performance.

For all SRAM cells, regardless of their writing structure, write delay is defined as the time taken for the Q node to reach 90% of V_{DD} when writing a '1' and 10% of V_{DD} when writing a '0'. Since our proposed 9T SRAM cell operates in a single-ended write mode, where writing a '1' is more challenging, we focus on comparing the write '1' delay across all SRAM cells. Figure 7 presents the write '1' delay of the SRAM cells at varying V_{DD} values. The conventional 6 T cell, with its differential structure and single access transistor, exhibits the lowest write delay. The HFWA9T and SB9T cells, employing a feedback-cutting technique, experience higher write delays.

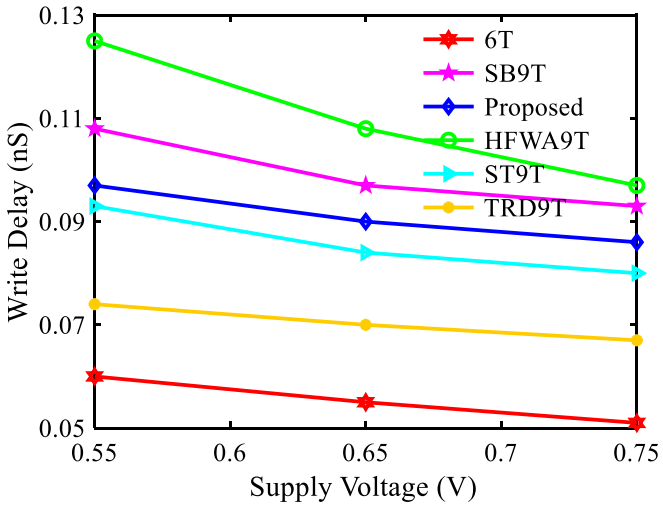

Figure 7. Write delay of investigated SRAM cells versus V_{DD}.

However, the stacked transistors in the HFWA9T's write path further increase its write delay. The TRD9T, utilizing transmission gates as its write switching access, performs write operations faster than the ST9T, which utilizes power gating and a hybrid cross-coupled structure. The proposed 9T SRAM cell, employing feedback-cutting and a TG in its access path, ranks fourth in terms of write delay. At $V_{DD} = 0.55$ V, it exhibits 1.63, 1.32, and 1.05 times higher write delay compared to the 6 T, TRD9T, and ST9T cells, respectively. However, it achieves a 9.23% and 21.60% reduction in write delay compared to the SB9T and WFWA9T cells, respectively.

3.4. Power consumption (Read/Write/Leakage)

Power consumption is a critical factor in SRAM cell design and optimization. A thorough understanding of the power components involved during hold, read, and write operations is crucial for minimizing energy usage. Efficient power management is particularly important in modern electronic systems where low power consumption is essential for extending battery life, reducing heat dissipation, and enhancing overall system performance [3].

The power consumed by an SRAM cell during hold, read, and write operations can be attributed to various factors, including leakage current, bitline switching activity, precharge circuit operation, and control signal transitions. Analyzing these power components allows designers to identify areas for optimization and develop strategies to minimize energy consumption [5].

SRAM cells with differential structures, like the 6 T cell, consume more power than single-ended cells due to their higher bitline switching activity. The SB9T, TRD9T, and HFWA9T cells, using two control signals during read operations, dissipate more power than the ST9T cell. However, the proposed 9T SRAM design, with read-path isolation and initially grounded-bitline BL, achieves the lowest read power. Write power consumption is influenced by the writing frequency. The proposed design's lower writing frequency leads to reduced write power dissipation.

Our findings shown in figures 8 and 9 demonstrate that the proposed 9T SRAM design achieves significant power reductions, with read power improved by 7.03% to 44.70% and write power reduced by 8.66% to 69.87%. This makes it an energy-efficient solution suitable for low-power applications.

Leakage power is a significant contributor to the overall power consumption of SRAM cells, especially in low-voltage and low-temperature environments. It arises from unwanted current flow through parasitic paths in the transistors, even when the cell is in a quiescent state. This leakage power can significantly impact the cell's energy efficiency and can be a major concern in battery-powered devices and high-density memory systems [25].

Figure 10 presents a comparison of leakage power across different SRAM cell designs at varying V_{DD} values. The conventional 6 T cell exhibits the highest leakage power due to its dual bitline structure lacking any leakage reduction techniques. The proposed designs, SB9T, HFWA9T, and ST9T, demonstrate lower leakage power compared to TRD9T, primarily due to their single-bitline structure. However, the ST9T cell, which incorporates a Schmitt-trigger inverter, introduces an additional leakage path. The leakage power equation for the proposed design was shown in equations (2) and (3). When the cell is holding '1' at Q, a non-zero possitive voltage developes at node X, which is due to the stack effect formed by TG and N3, wherein one side is connected to the ground (BL = '0') and another side is connected to V_{DD} (Q2 = '1'). This reduces the I_{sub} through transistors N3,

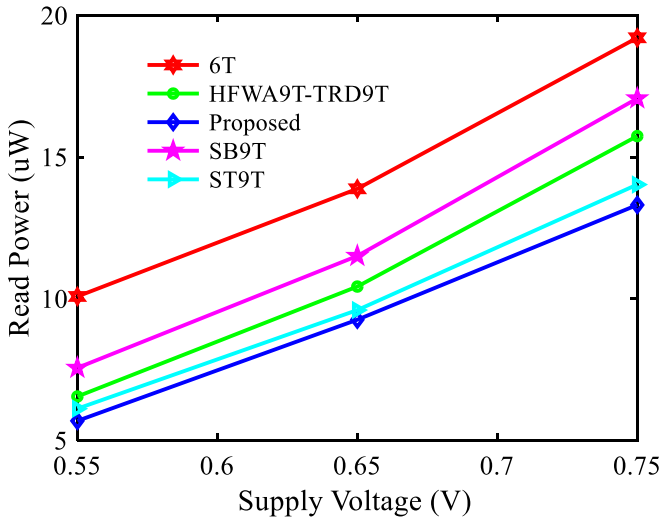

Figure 8. Read power of investigated SRAM cells versus V_{DD}.

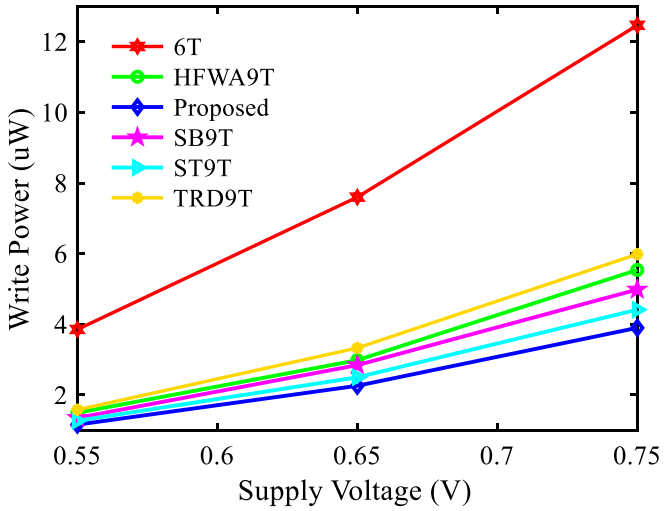

Figure 9. Write power of investigated SRAM cells versus V_{DD}.

N4, P4, and P5, and consequenctly the total leakage power reduces. As observed in figure 10, the proposed designs achieve a minimum improvement of 14.14% in leakage power at a V_{DD} of 0.55 V.

3.5. Process variation effect on static noise margin

Process variations, inherent in the manufacturing of integrated circuits, pose a significant challenge to the reliable operation of memory cells, particularly impacting their static noise margin (SNM). SNM is a critical parameter that measures the cell's ability to tolerate noise disturbances without causing errors during read or write operations [2]. Process variations introduce unpredictable deviations in the physical characteristics of transistors, leading to variations in their electrical parameters. Understanding and addressing process variation effects during the design phase is crucial for ensuring the robustness and reliability of memory cells [42, 43]. By incorporating strategies to mitigate these variations, designers can create memory systems that function reliably and consistently, even in the presence of noise and manufacturing uncertainties [1, 44].

Figures 11 and 12 respectively present the distribution plots for RSNM and WSNM for each studied SRAM cell. The conventional 6 T cell exhibits the highest RSNM variability due to its susceptibility to the read disturbance. However, it demonstrates acceptable WSNM variability thanks to its differential structure and single write-access transistor. The proposed design, incorporating read path isolation, feedback-cutting mechanisms, and transmission gate, exhibits enhanced robustness against process variations. This results in a significant reduction in RSNM variability by 63.96% and WSNM variability by 19.33% compared to the 6 T and HFWA9T SRAM cells, respectively.

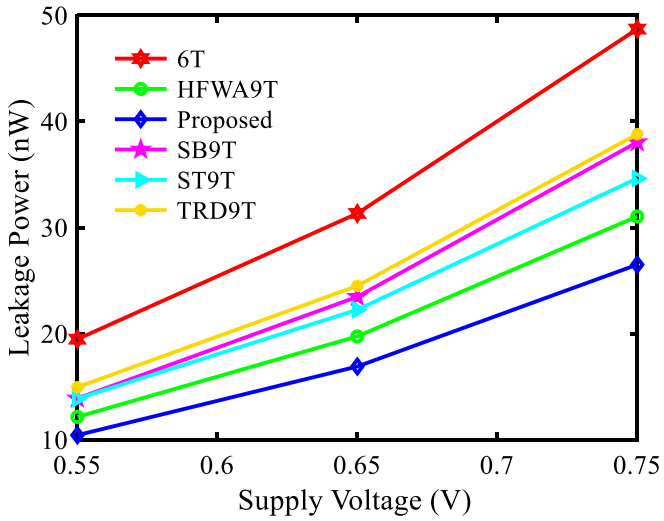

Figure 10. Leakage power of investigated SRAM cells versus V_{DD}.

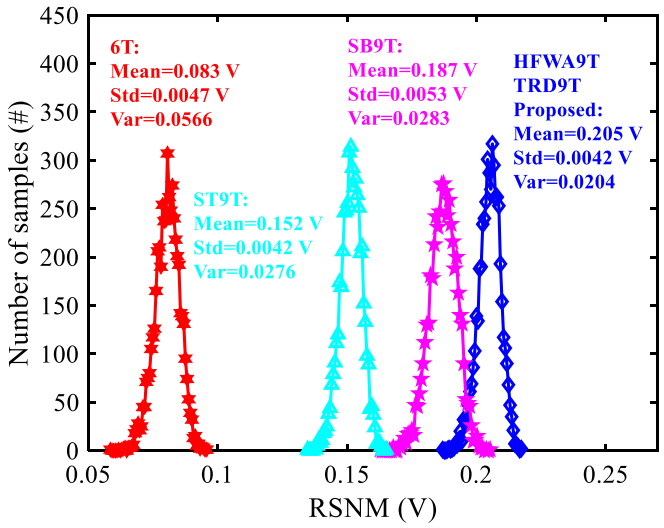

Figure 11. RSNM distribution plot of investigated SRAM cells at $V_{DD} = 0.55$ V.

3.6. Minimum operating voltage

The lowest possible voltage that an SRAM cell design can perform its hold/read/write operation reliably is called minimum operating volatge ($V_{DD\text{-}min}$) [45]. The $V_{DD\text{-}min}$ is the maximum value of hold-$V_{DD\text{-}min}$, read-$V_{DD\text{-}min}$, and write-$V_{DD\text{-}min}$, which are calculated at their 6-sigma. For hold and read operations, the hold-$V_{DD\text{-}min}$ and read-$V_{DD\text{-}min}$ are estimated when HSNM and RSNM are less than the thermal voltage (26 mV) and for write operation the write-$V_{DD\text{-}min}$ is estimated when WSNM is less than 0 V [45].

As can be seen in table 3, which gives the $V_{DD\text{-}min}$ value for SRAM cell designs under investigation, the conventional 6 T SRAM cell shows the highest $V_{DD\text{-}min}$. This is because the cell does not use a read-decoupled path and then expriences the read-disturbance issue. ST9T also experiences the read-disturbance issue but is able to mitigate it owing to using a combined cross-coupled structure of conventional and Schmitt-trigger inverters. Other SRAM cell design employ an isolated read path and a write-assist technique to improve RSNM and WSNM, respectively. This results in a decrease in $V_{DD\text{-}min}$ value.

3.7. A comperehensive summary of results

Table 4 provides a comprehensive comparison of the performance metrics of our novel SRAM cell design with other existing SRAM cell designs such as conventional 6 T [38], SB9T [24], ST9T [7], TRD9T [28], and HFWA9T [29] at 10 nm FinFET technology with $V_{DD} = 0.55$ V. Apart from the aforementioned SRAM cells, the simulation results for a power-gated 9 T (PG9T) SRAM cell [30] has also been added to table 4.

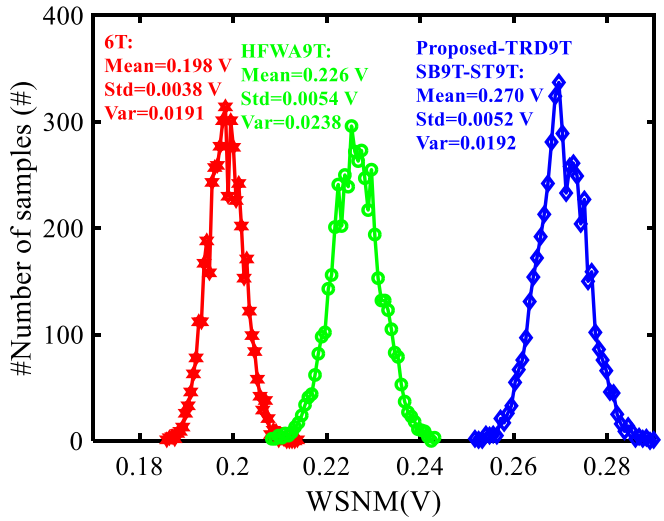

Figure 12. WSNM distribution plot of investigated SRAM cells at $V_{DD} = 0.55$ V.

Table 3. The $V_{DD\text{-}min}$ value for each SRAM cell under study.

Minimum operating voltage (V)	6 T [38]	HFWA9T [29]	SB9T [24]	TRD9T [28]	ST9T [7]	Prop. 9T (This work)
Hold-$V_{DD\text{-}min}$	310	310	317	310	340	310
Read-$V_{DD\text{-}min}$	535	310	317	310	410	310
Write-$V_{DD\text{-}min}$	385	280	265	265	270	265
$V_{DD\text{-}min}$	535	310	317	310	410	310

Table 4. Simulation results of different performance metrics for investigated SRAM cells at $V_{DD} = 0.55$ V.

SRAM cell design metrics	6 T [38]	HFWA9T [29]	SB9T [24]	TRD9T [28]	ST9T [7]	PG9T [30]	Prop. 9T (This work)
HSNM (mV)	208	208	208	208	197	205	208
RSNM (mV)	83	205	205	205	152	205	205
WSNM (mV)	187	226	270	270	270	226	270
Read delay (ns)	0.082	0.202	0.202	0.202	0.187	0.202	0.164
Read power (μW)	10.29	6.55	7.56	6.55	6.12	6.01	5.69
Write delay (ns)	0.06	0.125	0.108	0.074	0.093	0.112	0.098
Write power (μW)	3.85	1.49	1.35	1.58	1.27	1.24	1.16
Leakage power (nW)	19.48	12.16	13.9	14.96	13.88	10.28	10.44
Normalized EQM	1×	3.78×	4.38×	5.85×	5.07×	6.45×	12.23×

In order to show the overall performance of the investigated SRAM cell designs, which takes into account all the SRAM design metrics given in table 4, we have used an electrical quality metric (EQM) [46] (refer to equation (6)), as an SRAM figure of merit. As is evident from the last row of table 4, the proposed 9T SRAM cell design offers the highest EQM among all the compared SRAM cells, which makes it a good choice for use in applications whose need stable, lowe-power, and robust SRAM cell.

$$EQM = \frac{HSNM \times RSNM \times WSNM}{Read\_delay \times Write\_delay \times Read\_power \times Write\_power \times Leakage\_power} \tag{6}$$

4. Conclusion

The rapid evolution of the electronics industry necessitates the development of increasingly compact, high-speed, and energy-efficient memory technologies. While conventional MOSFET transistors have served as the cornerstone of memory design, their limitations become apparent as circuit dimensions shrink. FinFET transistors, with their exceptional performance and efficiency, offer a compelling alternative.

This paper unveils a groundbreaking 9T SRAM cell, meticulously designed and simulated using cutting-edge 10 nm FinFET devices at 0.55 operating voltage. This innovative design pushes the boundaries of memory performance, achieving remarkable improvements in stability and power consumption.

By strategically incorporating read path isolation and feedback-cutting techniques, the proposed cell boasts an impressive 1.10 (1.19) times improvement in read stability (writability) compared to conventional designs. And that's not all—the cell significantly reduces power consumption, with read power, write power, and leakage power dropping by at least 7.03%, 8.66%, and 14.14%, respectively. This efficiency is achieved through a clever combination of a single-bitline structure, stacked transistors in access paths, and optimized control signal assertion.

But the benefits extend beyond sheer performance. The proposed cell demonstrates remarkable resilience to manufacturing variations, exhibiting significantly lower variability in read stability and writability metrics. This robustness ensures reliable operation even in the face of unavoidable manufacturing imperfections.

This novel 9 T SRAM cell represents a significant leap forward in memory technology, paving the way for a future where devices are faster, more energy-efficient, and more reliable than ever before.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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