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RESEARCH ARTICLE-ELECTRICAL ENGINEERING

Innovative Transformerless Single-Phase Inverter for Minimizing Leakage Current and Enhancing Reactive Power in Grid-Tied PV Systems

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Abstract

Transformerless inverters are rapidly gaining popularity in small-scale grid-connected PV systems due to their compact size, cost-effectiveness, and superior efficiency compared to traditional inverters. However, leakage current caused by the stray capacitance between the direct current (DC) and alternating current (AC) circuits remains a challenge. To address this issue, various techniques such as using low leakage capacitors and adding inductors to the circuit have been developed. The inverter topology proposed in this paper changes DC power from solar panels into AC power and supplies it directly to the grid. Additionally, it keeps grid voltage and current total harmonic distortions (THDs) below 1%, reduces leakage current to nearly zero, and significantly improves power quality and reactive power. Moreover, with a consistent common-mode voltage, the leakage current has been effectively reduced to 1.084 mA. In the proposed configuration, there are five insulated gate bipolar transistors (IGBTs) and one reverse blocking insulated gate bipolar transistor (RBIGBT) utilized alongside an LCL filter. Also, the efficiency value has reached 99.77% in simulation phase, and it shows 98.16% in laboratory phase, which are an incredible value for this structure. The paper concludes that the proposed transformerless inverter offers a promising solution to address the challenges faced by photovoltaic (PV) systems while maintaining high efficiency and low cost. The validity of this topology has been confirmed through both MATLAB/Simulink simulations and physical implementation in the laboratory, with the simulation results aligning with the real-world performance.

Keywords Transformerless inverter · Leakage current suppression · Grid-tied photovoltaic systems · Reactive power capability · High-efficiency inverter topology

Abbreviations

DC	Direct current
AC	Alternating current
THD	Total harmonic distortion
PV	Photovoltaic
$RBIGBT$	Reverse blocking insulated gate bipolar transistor
$IGBT$	Insulated gate bipolar transistor
CM	Common mode

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FC	Flying capacitor
$HB\text{-}FC$	H-bridge flying capacitor
$HERIC$	Highly efficient reliable inverter concept
$M-NPC$	Mixed-voltage neutral point clamped
$SC-HB$	Split capacitor H-bridge
L	Filter inductance
C	Filter capacitance
V_{MPP}	Voltage at maximum power point
V_{OC}	Open-circuit voltage
P	Rated power
N_s	Number of series cell
f_s	Switching frequency
PRC	Proportional resonant controller
ω_c	Cutoff frequency
$HBZVR$	H-bridge zero-voltage state rectifier
$BDGOA$	Bio-dynamics grasshopper optimization algorithm
$DCSA$	Diligent crow search algorithm
$ZVT-HERIC$	Zero-voltage transition-highly efficient reliable inverter concept
DM	Differential mode
V_{CM}	Common-mode voltage
V_{DM}	Differential mode voltage
V_g	Grid voltage
I_g	Grid current
V_{pv}	Photovoltaic voltage
$P\&O$	Perturbation and observation
PI	Proportional integral
C_{PV1}, C_{PV2}	Photovoltaic capacitances (stray capacitances)
Q_{ref}	Reference reactive power
I_{ref}	Reference current
P_{MPP}	Power at maximum power point
I_{MPP}	Current at maximum power point
I_{SC}	Short-circuit current
V_{dc}	Input voltage
f_g	Grid frequency
C_1, C_2	DC-link capacitances
PM	Phase margin
ω_1	Angular frequency

1 Introduction

The advantages of voltage–source inverters in distributed grid-tied PV systems, including their low cost, proportional size, high efficiency, easy control, and advanced technology, make them more suitable and desirable for photovoltaic applications. Transformerless inverter structures have been proposed to enhance the performance and compatibility of grid-connected photovoltaic systems. These designs aim to improve the overall efficiency of the systems [1, 2]. PV systems play pivotal roles in energy markets. Recently, scientists have focused on PV systems that address challenges and improve their performance. These studies explore advanced methods for optimizing photovoltaic (PV) power prediction and industrial process control. The M5P model tree enhances PV output forecasting with improved accuracy and simplicity [3], while the bio-dynamics grasshopper optimization algorithm (BDGOA) and diligent crow search algorithm (DCSA) efficiently identify PV cell parameters [4, 5]. Additionally, the TDn(1 + PIDn) controller, optimized via the diligent crow search algorithm (DCSA), ensures precise pressure regulation in steam condensers [6].

Inverters are categorized into stand-alone and grid-connected types [7]. Within grid-connected inverters, there are two main types: transformerless and transformer-connected. Transformer-connected inverters have three primary drawbacks: they are costly, heavy, and can introduce harmonic distortion into the grid, which increases the total harmonic distortion (THD) of grid voltage and current. These issues have led to a decline in their popularity, while transformerless inverters are gaining favor as technology advances and the demand for more efficient solutions grows [8]. In recent years, the use of single-phase transformerless inverters in grid-tied PV systems has gained popularity due to their higher efficiency, smaller size, and lower cost compared to transformer-based inverters. However, transformerless inverters suffer from high leakage current, which can lead to safety hazards and degradation of the insulation of the PV module [9, 10]. On the other hand, there is one problem with transformerless inverters that are commonly grounded, namely that leakage current flows through the stray capacitors and the ground lines [11, 12]. As a result, there is a potential safety risk involved. Therefore, several research studies have focused on developing techniques to reduce the leakage current and improve the performance of transformerless inverters [13]. The use of multilevel transformerless inverters is crucial in optimizing the performance and efficiency of single-phase low-power photovoltaic systems. Zhu et al. [14] proposed a new single-phase five-level transformerless inverter designed for photovoltaic applications. Proposed inverter uses two freewheeling paths to maintain the common-mode (CM) voltage at a constant level, reducing the leakage current below 300 mA, in compliance with the VDE-0126–1-1 standard. This proposed topology has several advantages over conventional H-bridge flying capacitor (HB-FC) topology, including stabilized flying capacitor (FC) voltages at $\frac{V_{dc}}{4}$, leading to reduced costs of passive components and higher efficiency due to the use of low-voltage stress devices. Hosseinkhani et al. [15] introduce an innovative inverter that enhances output voltage efficiency and minimizes leakage current. Their study compares this

new topology with highly efficient reliable inverter concepts (HERICs) and mixed-voltage neutral point clamped (M-NPC) inverters. The findings indicate that the proposed inverter is superior in reducing output current total harmonic distortion compared to HERIC and M-NPC. In addition, the new inverter features five output voltage levels, which contributes to its greater efficiency compared to competitors with only three levels. Despite the complexity of its structure and switching, the proposed topology offers significant advantages, including voltage stabilization in common-mode and reduced leakage currents. Kalathi et al. [16] present a novel transformerless approach for grid-tied photovoltaic (PV) systems. Their design incorporates a MOSFET switch that ensures high efficiency even with the addition of reactive power to the grid. The circuit topology minimizes leakage current by maintaining the common-mode (CM) voltage at a balanced level. Additionally, the absence of pulse width modulation dead time helps reduce harmonic distortion. Azri et al. [17] proposed a transformerless inverter featuring a DC-link capacitor balancing circuit, known as the split capacitor-H-bridge (SC-HB) inverter. This SC-HB topology maintains a nearly constant common-mode voltage and reduces leakage ground current. Both simulation and experimental results show that the SC-HB inverter offers higher efficiency and lower grid current ripple compared to traditional H-bridge inverters. These advantages make it an attractive option for power conversion in transformerless grid-connected photovoltaic (PV) systems. Shahabadini et al. [18] proposed a multilevel cascaded H-bridge inverter and employed a novel modulation technique to reduce leakage current. Biswas et al.[19] presented a highly efficient new topology for transformerless inverters, although it does not effectively address leakage current. In contrast, Vázqueet al. [20] introduced a novel common-mode inverter topology that connects the grid neutral line to the negative terminal of the PV system to reduce leakage current. They use a sliding mode controller to manage the system. Jahan et al. [21] presented novel H9 and H10 transformerless solar PV inverters designed to reduce leakage current and harmonic distortion, enhancing the efficiency in the solar power systems, and Li et al. [22] proposed an H-bridge topology called as H5 topology with low leakage current. Khan et al. [23] presented an overview of various conventional topologies, including H6, oH5, H5, HERIC, H-bridge zero-voltage state rectifier (HBZVR), and HBZVR-D, is provided. Among these, the HERIC topology is highlighted for its high efficiency and acceptable leakage current reduction, while H5 is valued for its simplicity and lower cost. Each design offers a balance between efficiency, complexity, and cost, making them suitable for different photovoltaic applications.

In order to isolate the PV array from the grid, switches have been integrated into existing topologies. For example, the H5 topology includes a switch between the input and the bridge arms, as discussed in [24]. Another topology, the oH5 builds upon the H5 topology by adding a switch branch between the input and the midpoints of bridge arms [25]. The family of H6 topologies adds two switches between the input and the bridge arms or integrates them into the bridge arms [26, 27]. In the family of HERIC topologies, an extra freewheeling branch is added between the bridge arm and filter inductors [28]. The key findings from the other remarkable researches are summarized in Table 1.

1.1 Research Gap and Contributions

Despite significant advances in transformerless inverter technology for grid-connected photovoltaic systems, challenges remain, particularly in terms of reducing leakage current and improving system efficiency and power quality. Previous research has proposed various topologies and modulation techniques to address these issues, such as multilevel transformerless inverters and innovative switch configurations. While these structures have shown good benefits, most of them include complex structures and require additional components, which can increase the overall cost and complexity of the system. In addition, although some topologies such as H5, HERIC, and SC-HB have shown acceptable performance in reducing leakage current and increasing efficiency, there is still a need for simpler and more cost-effective solutions that maintain current performance standards output or provide more effective for grid-connected PV systems.

The new inverter topology proposed in our study introduces a transformerless design that uses improved modulation techniques and RBIGBT switches to effectively reduce leakage current, increase efficiency, and provide reactive power with a minimal harmonic distortion. This new approach seeks to bridge the gap by providing a less complex and more efficient solution that addresses the economic and technical limitations of existing inverter designs for grid-connected PV systems. The most important contributions of this research are:

- *Innovative Transformerless Inverter Topology* By integrating a new RBIGBT switch within the H5 topology, this advanced design creates a powerful inverter structure. It significantly reduces leakage currents and boosts overall efficiency, eliminating the need for a traditional transformer. This innovative topology is specifically engineered to enhance grid-connected photovoltaic systems.
- *Minimizing leakage current* The proposed inverter solves the problem of leakage current by maintaining a constant CM voltage and brings the amount of leakage current to values close to zero and displays a desirable result. In this structure, advanced modulation strategies are used along with RBIGBT switches to effectively divide the input

Table 1 Overview of specifics in the several studied inverter topologies

Ref	Proposed inverter topology	Reactive power capability	Efficiency %	Advantages	Disadvantages
[29]	Common-Ground	Yes	99.20	No common-mode effect observed, fewer semiconductor devices needed, smaller filter necessary	Managing flying capacitor, switched capacitor, or flying inductor control poses challenges
[11]	HERIC Active 2	Yes	97	Constant common-mode voltage and low common-mode current	Additional semiconductor components required
[30]	ZVT-HERIC	Yes	97.6	Minimal conduction losses, minimum (THD)	Extra switches needed; presence of residual line frequency leakage current
[31, 32]	H6-ANPC	No	–	Maintain constant common-mode voltage, resulting in reduced leakage current	Cannot effectively reduce leakage current requirement of large number of gate driver signals
[33, 34]	Improved H6	No	97.76	Effectively reduces leakage current and the total harmonic distortion (THD) of grid voltage and current	Primary limitation of this topology is that it has higher conduction loss

voltage into two equal parts. This innovative approach isolates the inverter from the PV array in zero-voltage states, thereby reducing the leakage current to almost zero.

- *Increased system efficiency* With this innovative approach, the system efficiency reaches an impressive 99.77% in simulations and 98.16% in experimental tests, demonstrating the effectiveness and operational excellence of the proposed inverter structure in grid-connected applications.
- *Reactive power capability* The proposed topology is able to provide reactive power to the network, which increases its performance and flexibility in different network scenarios.
- *Harmonic Distortion Reduction* The proposed topology produces a three-level output voltage that significantly reduces current total harmonic distortion (THD) to 0.76%. This improvement ensures higher power quality and better compliance with network standards.

By addressing these key specifications, the proposed inverter structure not only increases performance and efficiency but also contributes to the development of more reliable and cost-effective grid-connected PV systems.

The paper is organized as follows: Section 2 introduces the proposed topology and modulation strategy. Section 3 provides an analysis of the proposed topology. Section 4 presents the control mechanism employed in the proposed topology. Section 5 details the simulation and experimental setup and results, and finally, Sect. 6 concludes the paper.

2 Proposed Topology

2.1 Structure and Modulation Technique Description

The proposed topology is presented in Fig. 1a. In addition, the modulation strategy for H5 is illustrated in Fig. 1b. To investigate the reactive power capability of an inverter structure and produce a three-level unipolar voltage, a modification of its operation into eight modes is required. The initial four modes correspond to unity power factor operation, where the grid voltage and current maintain identical polarities. On the other side, the remaining four modes pertain to post-phase or pre-phase power factor, where the grid voltage and current exhibit opposite polarities, resulting in negative power transfer. These findings have significant implications for the design and optimization of inverter systems, particularly in the context of renewable energy integration and grid stability. The phenomenon of zero-voltage states occurs when the voltage of the main power supply is positive, while the current is negative. In operation mode VI, the switches S_2, S_3, S_4, and S_5 are non-conductive, remaining in the off state, with the exception of S_1 which is in the on state. Similarly, during operation mode VIII, S_1, S_3, S_5, and S_5 are non-conductive, while S_2 is in the on state.

This configuration, depicted in Fig. 2a and b, results in a lack of any available path for the flow of electrical current. As a consequence, achieving zero-voltage states is unattainable. The analysis shows that during negative power flow in

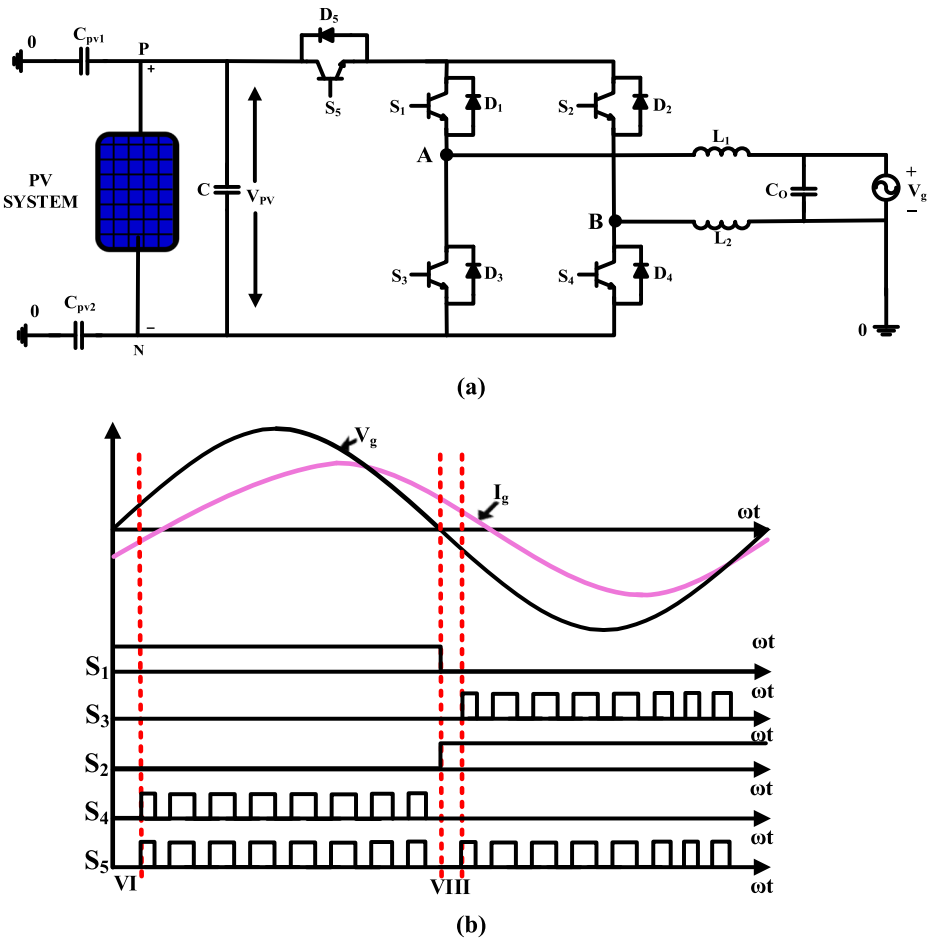


Fig. 1 Topology of H5 (**a**) and switching waveforms (**b**)

modes VI and VIII, it is impossible to reach a zero-voltage state because the current has no path. Consequently, there are leakages of current from PV inverters into the grid, and this results in THDs being injected into the system. The conventional modulation strategy only switches S_1 and S_2 during the network frequency, but during negative power flow, only these switches remain on, and no current flows during the freewheeling period [23]. Furthermore, other structures with conventional modulation strategies do not provide any path for current to flow in the negative power region, rendering them unsuitable for reactive power applications. To address this issue, an improved modulation strategy is proposed to establish a bidirectional flow path during the freewheeling period and achieve reactive power handling capability.

Upon careful analysis, it has been determined that the H5 topology utilizing the conventional modulation strategy fails to effectively regulate the reactive power [23, 35]. As a result, an alternative modulation technique has been developed, as depicted in Fig. 3 that is capable of generating zero-voltage states in modes VI and VIII. This approach offers a path for the freewheeling current during negative power flow, which is not possible using the traditional modulation strategy. The revised modulation strategy of the proposed topology is depicted in Fig. 3.

During operational mode VI, the system activates only the S_1 and S_2 switches, while the remaining switches are deactivated. This configuration results in the generation of zero-voltage levels. Figure 4a illustrates the current path during freewheeling periods in this operational mode. The current flows throughL_2, the grid,L_1, S_2, and anti-parallel diodeD_1. In the subsequent state VIII, the system operates with a different set of switches activated and deactivated. The S_1 and S_2 switches are simultaneously activated, while theS_3, S_4, and S_5 switches remain off. Figure 4b illustrates the current path during freewheeling periods in this state. The current flows throughL_1, the grid,L_2, S_1, and anti-parallel diodeD_2. Based on the analysis of the results, an improved topology for managing V_{CM} and V_{DM} is recommended for stages VI and VIII of the grid-connected PV system. The proposed topology is detailed as follows:

$$V_{CM(VI)} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \tag{1}$$

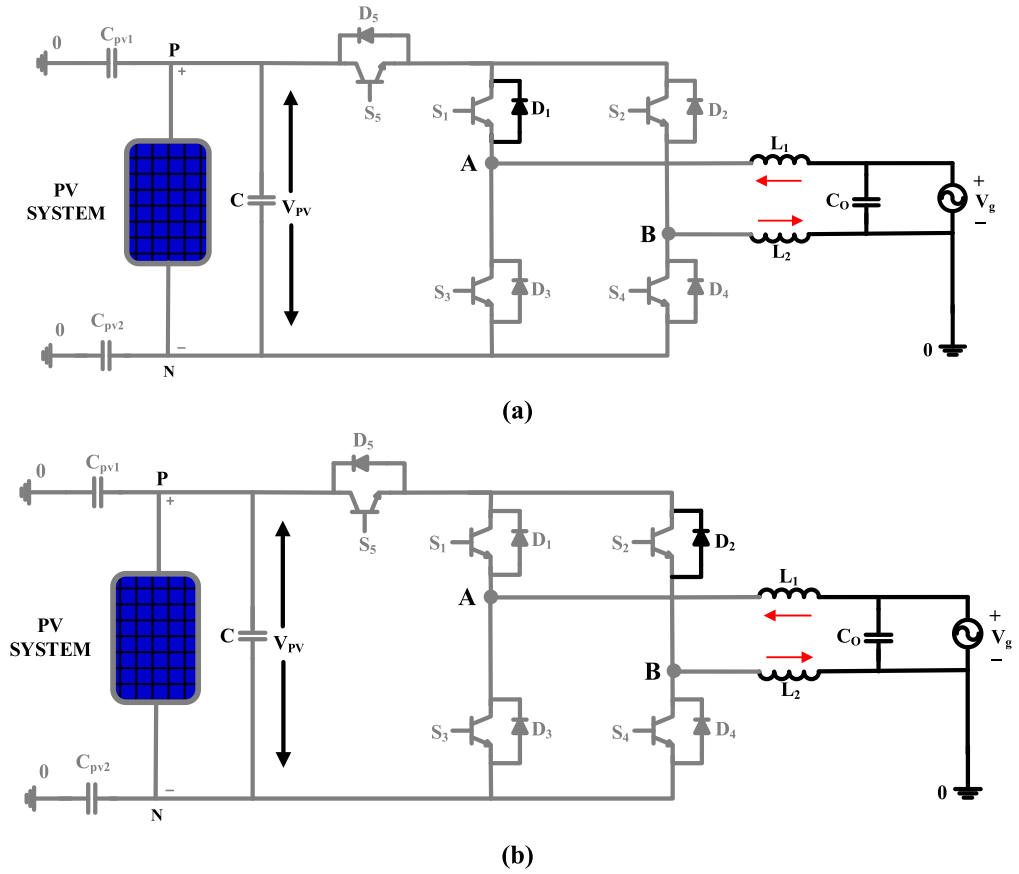


Fig. 2 Operation during freewheeling periods in the negative power region, showing **a** positive grid voltage with negative grid current and **b** negative grid voltage with positive grid current

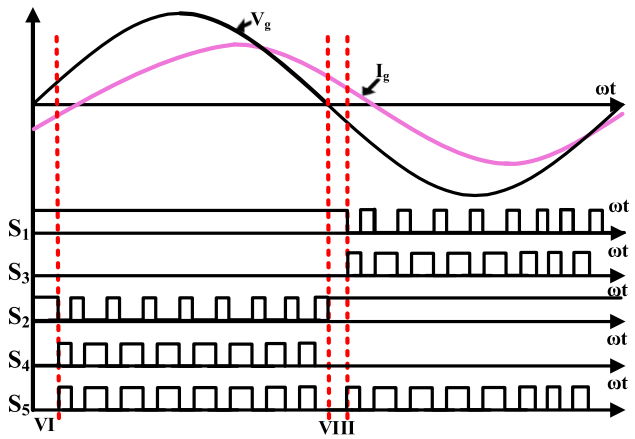


Fig. 3 Switching waveforms of the proposed modified modulation

$$V_{DM(VI)} = V_{AN} - V_{BN} = 0 \tag{2}$$

$$V_{CM(VIII)} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \tag{3}$$

$$V_{DM(VIII)} = V_{AN} - V_{BN} = -V_{PV} \tag{4}$$

3 Analysis of the Proposed Topology

The proposed inverter for use in grid-connected PV systems is illustrated in Fig. 5. The inverter features a bidirectional switch comprising two RBIGBT switches, S_6 and S_7, arranged in reverse parallel. This setup allows for the input voltage to be evenly divided into two parts and enables precise voltage control on the DC-link capacitors, C_1 and C_2. Additionally, the inverter includes four full-bridge topology switches, S_1, S_2, S_3, and S_4, which play a critical role in the power conversion process from the PV system to the grid. The network separator switch, S_5, positioned between the negative DC terminal and the full bridge, as a grid separator.

3.1 Operational Modes and Reactive Power Capability

The inverter's operation is divided into eight distinct modes, as shown in Fig. 6, to achieve a unipolar three-level voltage output and assess its reactive power handling capabilities. Each mode's functioning is described in detail below.

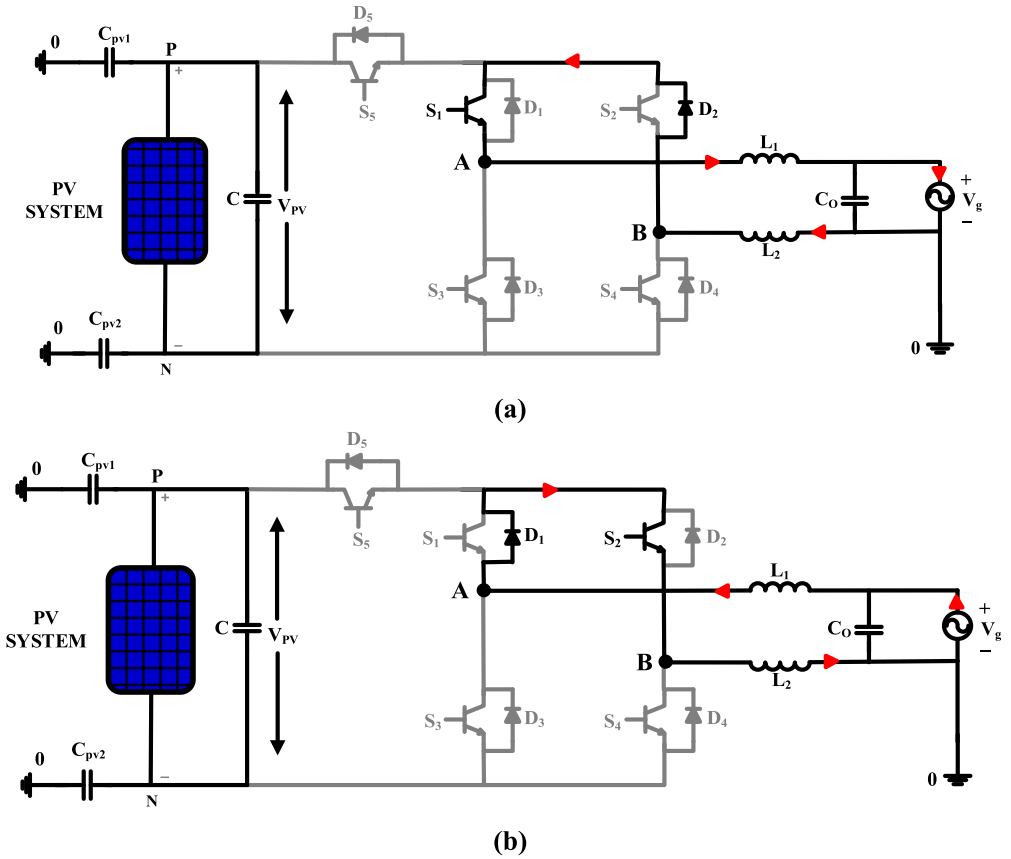


Fig. 4 Operation during freewheeling periods VI and VIII using a modified modulation technique, showing **a** positive grid voltage with negative grid current and **b** negative grid voltage with positive grid current

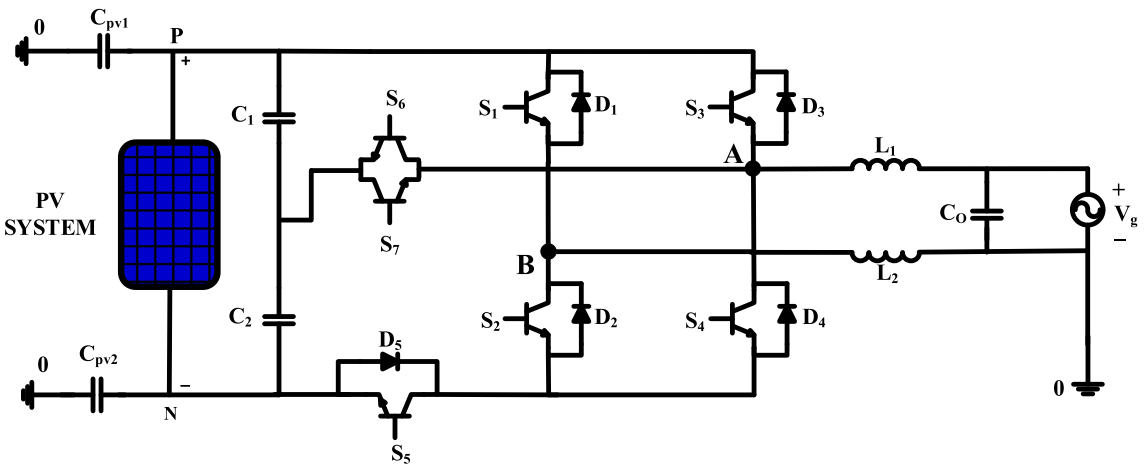


Fig. 5 Proposed topology

3.1.1 Mode I: Positive Grid Voltage and Positive Grid Current

The state of the switches can be described as follows: S_2, S_3, and S_5 are turned on, while S_1, S_4, and the clamping branch switch RBIGBT are turned off. As a result, the current follows a path through S_3, L_1, the grid, L_2, S_2, and S_5, as illustrated in Fig. 7a. The voltage values $V_{AB} = V_{PV}, V_{AN} = V_{PV}$, and $V_{BN} = 0$. Consequently, the CM and DM voltages are determined as follows:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{PV} + 0}{2} = \frac{V_{PV}}{2} \tag{5}$$

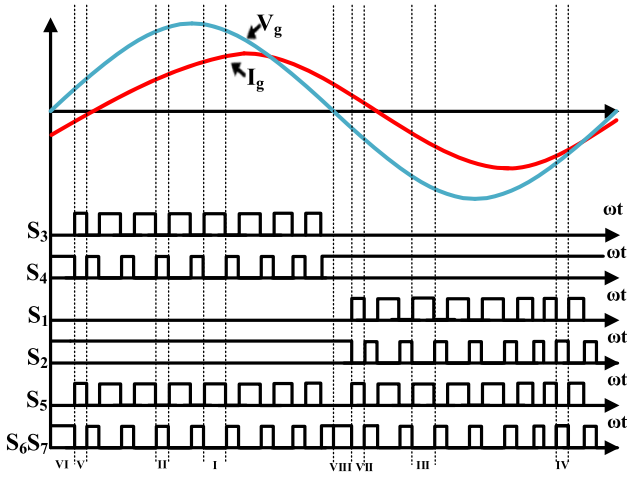


Fig. 6 Switching waveforms of the proposed topology

$$V_{DM} = V_{AN} - V_{BN} = V_{PV} \tag{6}$$

3.1.2 Mode II: Freewheeling Mode with Positive Grid Voltage and Positive Grid Current

In this mode, switches S_1, S_3, and S_5 are turned off, while switches S_2, S_4, and RBIGBT are activated. Consequently, the current flows in a freewheeling path through L_1, the grid, L_2, the anti-parallel diode D_4, and switch S_2, as illustrated in Fig. 7b. The terminal voltages V_{AN} and V_{BN} are clamped to $\frac{V_{PV}}{2}$ by the RBIGBT switch. The voltage values are as follows: $V_{BN} = 0$, $V_{AN} = \frac{V_{PV}}{2}$, and $V_{BN} = \frac{V_{PV}}{2}$. Therefore, the CM and DM voltages can be determined as:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \tag{7}$$

$$V_{DM} = V_{AN} - V_{BN} = 0 \tag{8}$$

3.1.3 Mode-III: Grid Voltage and Grid Current are Negative

Switches S_2, RBIGBT and S_3 are in the off state, while switches S_1, S_4 and S_5 are turned on. Consequently, the current flows through S_4, S_5, L_2, the grid, L_1, and S_1, following the direction shown in Fig. 8a. These voltage values are $V_{AB} = -V_{PV}$, $V_{AN} = 0$, and $V_{BN} = V_{PV}$. Therefore, the corresponding CM and DM voltages can be calculated as follows:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \tag{9}$$

$$V_{DM} = V_{AN} - V_{BN} = -V_{PV} \tag{10}$$

3.1.4 Mode IV: Freewheeling Mode with Negative Grid Voltage and Negative Grid Current

Switches S_1, S_3, and S_5 are turned off, whereas switches S_2, S_4, and RBIGBT are turned on in this scenario. As a result, the current flows in a freewheeling mode through L_2, the grid, L_1, the anti-parallel diode D_2, and S_4, as illustrated in Fig. 8b.

The switch RBIGBT clamps the terminal voltages V_{AN} and V_{BN} to $\frac{V_{PV}}{2}$. The voltage values are $V_{AB} = 0$, $V_{AN} = \frac{V_{PV}}{2}$, and $V_{BN} = \frac{V_{PV}}{2}$, which leads to the following CM and DM voltages.

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \tag{11}$$

$$V_{DM} = V_{AN} - V_{BN} = 0 \tag{12}$$

3.1.5 Mode V: Positive Grid Voltage and Negative Grid Current

During the negative power region, the current flows through anti-parallel diode D_5 of switch S_5, anti-parallel diode D_2 of switch S_2, L_2, the grid, L_1, and anti-parallel diode D_3 of switch S_3, following the path depicted in Fig. 9a. The voltage values are $V_{AB} = V_{PV}$, $V_{AN} = V_{PV}$, and $V_{BN} = 0$. Based on these voltage values, the corresponding CM and DM voltages can be calculated as follows:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{PV} + 0}{2} = \frac{V_{PV}}{2} \tag{13}$$

$$V_{DM} = V_{AN} - V_{BN} = -V_{PV} \tag{14}$$

3.1.6 Mode VI: Freewheeling Mode with Positive Grid Voltage and Negative Grid Current

In this circuit configuration, switches S_2, S_4, and RBIGBT are turned on, while switches S_1, S_3, and S_5 are turned off. To generate a zero-voltage state, the current flows through L_2, the grid, L_1, and the anti-parallel diode D_2 of switch S_2, following the path illustrated in Fig. 9b. The switch RBIGBT clamps the terminal voltages V_{AN} and V_{BN} to $\frac{V_{PV}}{2}$.

The voltage values in this case are $V_{AB} = 0$, $V_{AN} = \frac{V_{PV}}{2}$, and $V_{BN} = \frac{V_{PV}}{2}$, which allow for the calculation of the corresponding CM and DM voltages as:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \tag{15}$$

$$V_{DM} = V_{AN} - V_{BN} = 0 \tag{16}$$

3.1.7 Mode VII: Negative Grid Voltage and Positive Grid Current

In this mode of operation, the current freewheels through the anti-parallel diode D_5 of switch S_5, L_1, the grid, L_2, the anti-parallel diode D_4 of switch S_4, and the anti-parallel diode D_1 of switch S_1, following the path shown in Fig. 10a.

The voltage values in this configuration are $V_{AB} = -V_{PV}, V_{AN} = 0$, and$V_{AN} = -V_{PV}$, which enable the calculation of the corresponding CM and DM voltages as:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \tag{17}$$

$$V_{DM} = V_{AN} - V_{BN} = -V_{PV} \tag{18}$$

3.1.8 Mode VIII: Freewheeling Mode with Negative Grid Voltage and Positive Grid Current

The switches S_1, S_3, and S_5 are turned off, while switches S_2, S_4, and RBIGBT are turned on. To generate a zero-voltage state, the current flows through L_1, the grid, L_2, and the anti-parallel diode D_4 of switch S_4, as illustrated in Fig. 10b. The switch RBIGBT clamps the terminal voltages V_{AN} and V_{BN} to $\frac{V_{PV}}{2}$, and the voltage values in this mode are $V_{AB} = 0$, $V_{AN} = \frac{V_{PV}}{2}$, and $V_{BN} = \frac{V_{PV}}{2}$. By using these values, the corresponding CM and DM voltages can be determined as follows:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \tag{19}$$

$$V_{DM} = V_{AN} - V_{BN} = 0 \tag{20}$$

Finally, the proposed inverter administers to produce three levels of output voltages with levels of $+V_{PV}$, 0 and $-V_{PV}$. The summary of switching states and output voltage is given in Table 2.

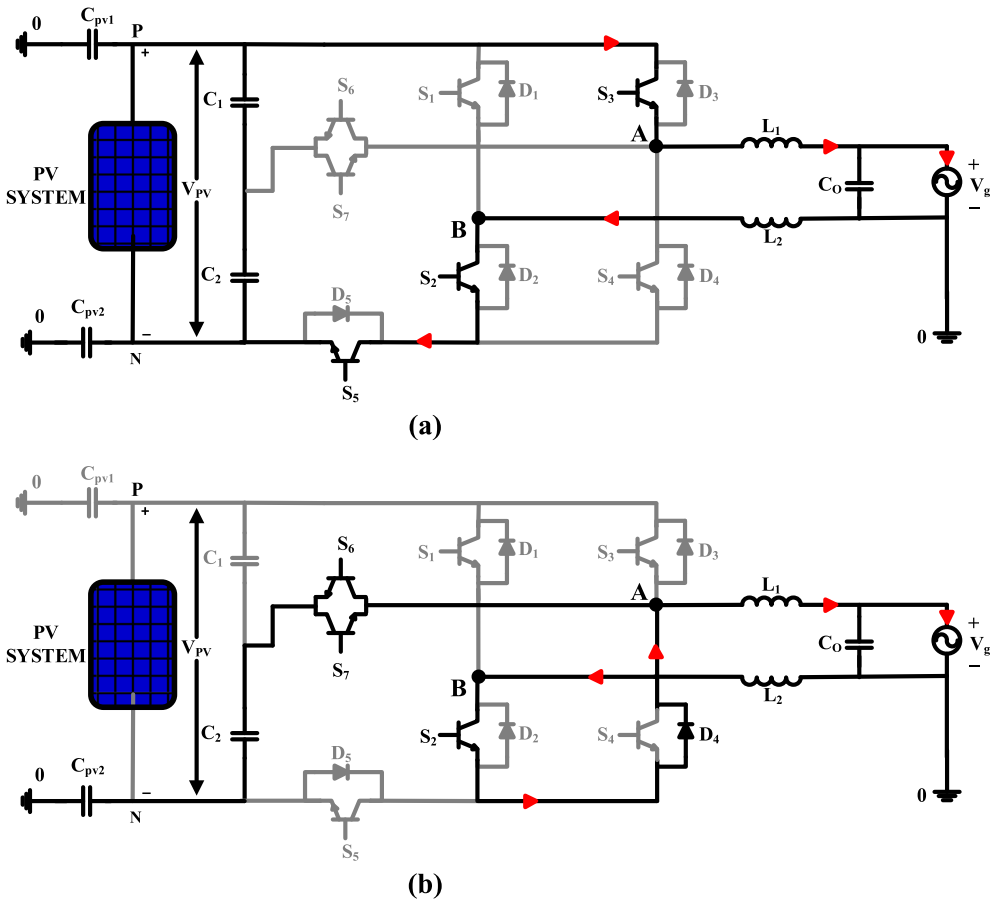


Fig. 7 Operating modes with positive grid voltage and positive grid current, showing **a** conduction mode and **b** freewheeling mode

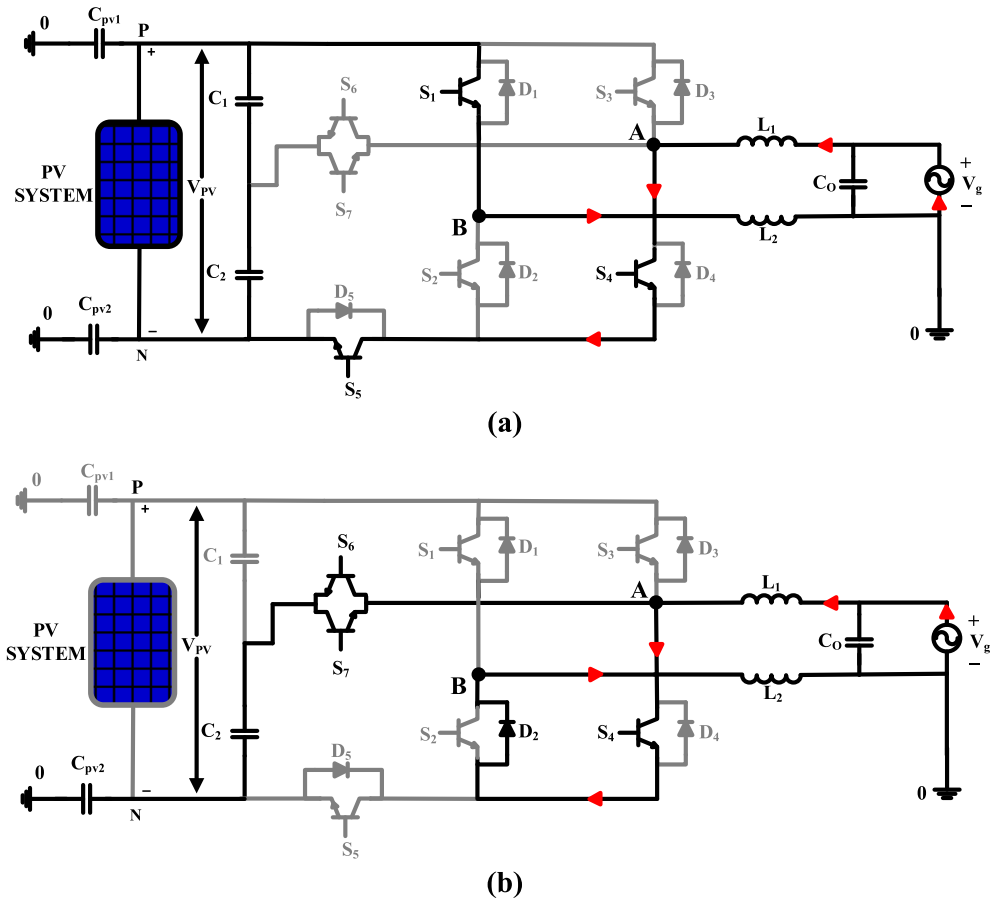


Fig. 8 Operating modes with negative grid voltage and negative grid current, illustrating **a** conduction mode and **b** freewheeling mode

4 Control Mechanism of the Proposed Topology

The block diagram of the control strategy in grid-tied PV system is shown in Fig. 11. The control strategy includes grid-connected current control, voltage control block diagram, and gate signals generation. Also, Fig. 12 shows control schematic of grid-connected PV system with proposed inverter. The detailed implementation method is described as follows.

4.1 Design of Voltage and Current Controller

Figure 13 illustrates the equivalent circuit of the system with control input u(t). The transfer function for the current and voltage controller and their open-loop transfer function are expressed, respectively, in Eqs. (21)–(26).

Current controller

$$G_{IU}(s) = \frac{I_g(s)}{V_{AB}(s)}\bigg|_{V_{g(s)=0}} \tag{21}$$

In addition, the equation for proportional resonant (PR) controller is following:

$$G_{PR}(s) = K_P + \frac{2 \times K_r \times \omega_{PRC} \times s}{s^2 + 2 \times \omega_{PRC} \times s + \omega_1^2} \tag{22}$$

By applying the PR controller to the open-loop transform function, the closed-loop transform function as shown in Fig. 14 is given as follows:

$$\begin{aligned} G_{OLC} &= G_{IU}(s) \times G_{PRC}(s) \\ &= \frac{V_{PV}}{L_s}\left[K_P + \frac{2 \times K_r \times \omega_{PRC} \times s}{s^2 + 2 \times \omega_{PRC} \times s + \omega_1^2}\right] \\ &= \frac{V_{PV}}{L_s}\left[\frac{K_P \times s^2 + 2 \times \omega_{PRC} \times (K_P + K_r) \times s + K_P \times \omega_1^2}{s^2 + 2 \times \omega_{PRC} \times s + \omega_1^2}\right] \end{aligned} \tag{23}$$

.

Voltage controller

$$G_{VI}(s) = \frac{V_{PV}(s)}{I_g(s)} = -\frac{1}{2 \times C_{pv} \times s} \tag{24}$$

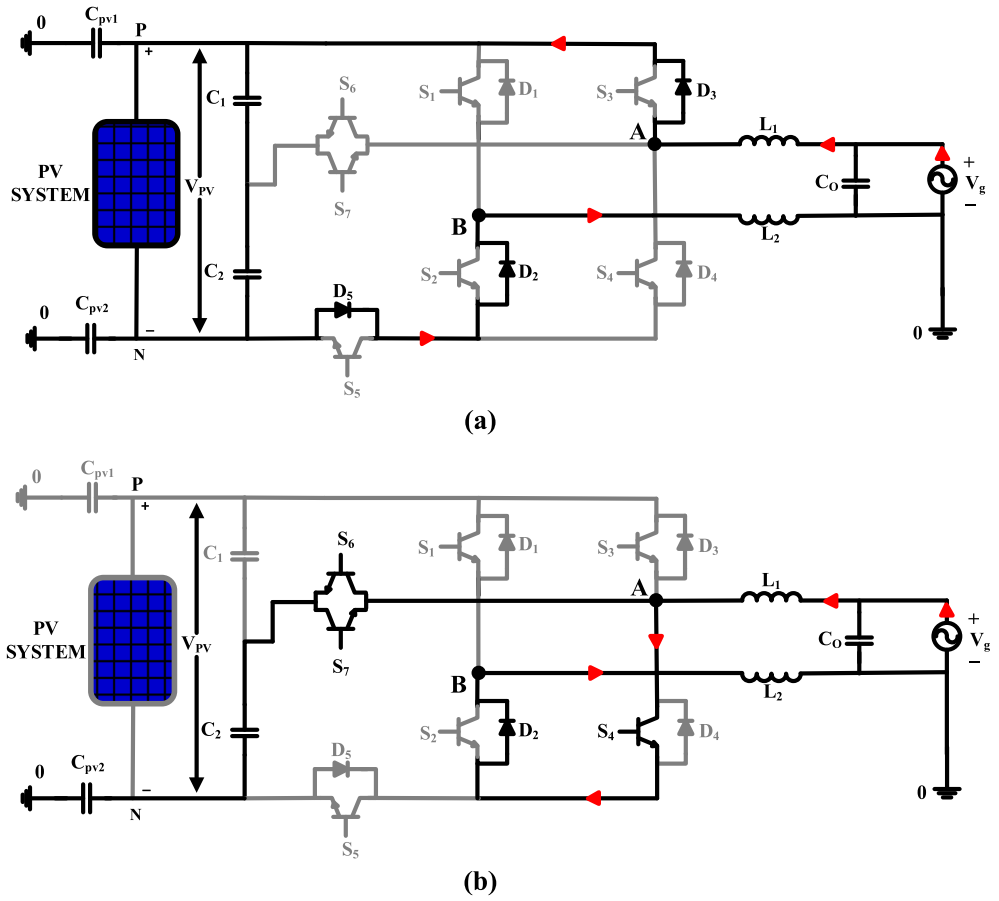


Fig. 9 Operating modes with positive grid voltage and negative grid current, showing **a** conduction mode and **b** zero-voltage state

In addition, the equation for PI controller is given by:

$$G_{PV}(s) = K_{PV} + \frac{K_{IV}}{s} \tag{25}$$

By applying the PI controller to the open-loop transform function, the closed-loop transfer function as shown in Fig. 15 is obtained as:

$$\begin{aligned} G_{OLV} &= G_{PV}(s) \times G_{VI}(s) \\ &= \left(K_{PV} + \frac{K_{IV}}{s}\right) \times \frac{1}{2 \times C_{pv} \times s} \\ &= \frac{K_{PV}}{2 \times C_{pv}} \times \frac{s + \frac{K_{IV}}{K_{PV}}}{s^2} \end{aligned} \tag{26}$$

To analyze the frequency response of the system, the Nyquist stability criterion must first be applied. Following are the conditions that must be met in order to satisfy the Nyquist criterion:

Condition (I)

At the cutoff frequency, the phase margin of the open-loop transfer function of the system should be greater than or equal to a certain angle ($\pi + \angle G_{OLC}(j\omega_c) = PM \geq \theta$). Different frequency values are considered as follows:

If $f_{PRC} = 0.5Hz$ so, $\omega_{PRC} = 2 \times \pi \times f_{PRC} = \pi rad/s$

If $f_1 = 50Hz$ so, $\omega_1 = 2 \times \pi \times f_1 = 100\pi rad/s$

If $f_C = 1kHz$ so, $\omega_C = 2 \times \pi \times f_C = 200\pi rad/s$

Additionally, because the speed of the voltage control loop is much slower than that of the current control loop, then we consider the cutoff frequency of the voltage loop to be $\frac{1}{20}$ of the current loop. Thus, we have:

$$\begin{aligned} f_C &= \frac{1}{20}(1\ kHz) = 50\ HZ \text{ so, } \omega_{CV} \\ &= 2 \times \pi \times f_{CV} = 100\pi\ rad/s \end{aligned}$$

For current control:

$$\alpha = \frac{2 \times \omega_{PRC} \times \omega_c}{\omega_1^2 - \omega_c^2} = \frac{4}{10 - 4000} = -0.001 \tag{27}$$

If the phase margin is considered to be 50°:

$$\begin{aligned} K_r \geqslant \frac{K_P}{\alpha} \times \left[\tan\left(PM - \frac{\pi}{2} + tan^{-1}(\alpha)\right) - 1\right] \\ = 1000 \times K_p \times \tan(40°) = K_r \geqslant 839K_p \end{aligned} \tag{28}$$

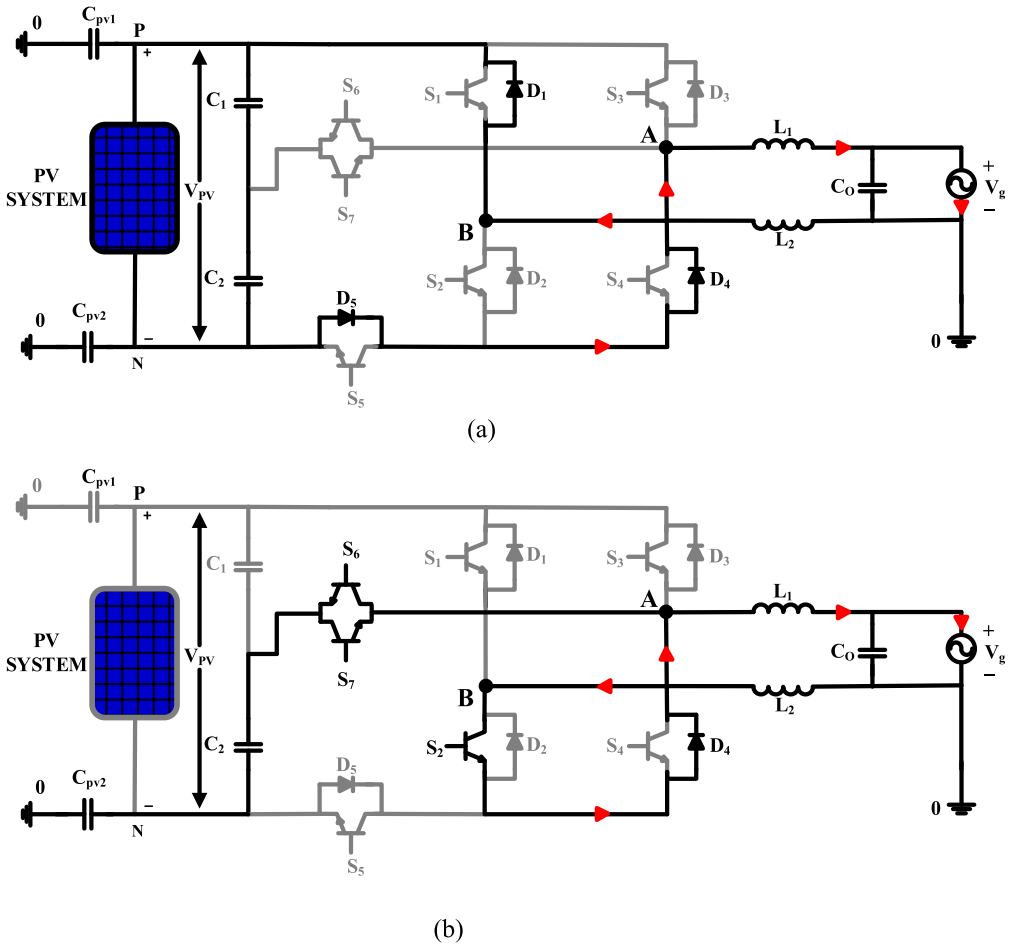


Fig. 10 Operating modes with negative grid voltage and positive grid current, illustrating **a** conduction mode and **b** zero-voltage state

Table 2 Overview of switching state and output voltage in proposed topology

Mode	Switching mode							Diode mode							Output voltage				
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	D_1	D_2	D_3	D_4	D_5	D_6	D_7	V_{AB}	V_{AN}	V_{BN}	V_{CM}	V_{DM}
I	off	on	on	off	on	off	off	off	off	off	off	off	off	off	$+V_{PV}$	$+V_{PV}$	0	$+V_{PV}/2$	$+V_{PV}$
II	off	on	off	off	off	on	on	off	off	off	on	off	off	off	0	$+V_{PV}/2$	$+V_{PV}/2$	$+V_{PV}/2$	0
III	on	off	off	on	on	off	off	off	off	off	off	off	off	off	$-V_{PV}$	0	$+V_{PV}$	$+V_{PV}/2$	$-V_{PV}$
IV	off	off	off	on	off	on	on	off	on	off	off	off	off	off	0	$+V_{PV}/2$	$+V_{PV}/2$	$+V_{PV}/2$	0
V	off	off	off	off	off	off	off	off	on	on	off	on	off	off	$+V_{PV}$	$+V_{PV}$	0	$+V_{PV}/2$	$+V_{PV}$
VI	off	off	off	on	off	on	on	off	on	off	off	off	off	off	0	$+V_{PV}/2$	$+V_{PV}/2$	$+V_{PV}/2$	0
VII	off	off	off	off	off	off	off	on	off	off	on	on	off	off	$-V_{PV}$	0	$+V_{PV}$	$+V_{PV}/2$	$-V_{PV}$
VIII	off	on	off	off	off	on	on	off	off	off	on	off	off	off	0	$+V_{PV}/2$	$+V_{PV}/2$	$+V_{PV}/2$	0

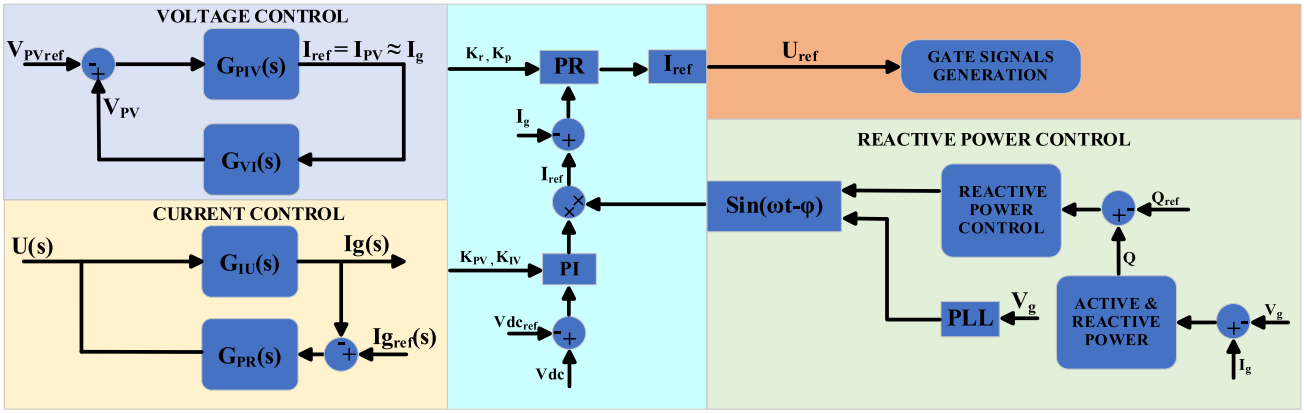
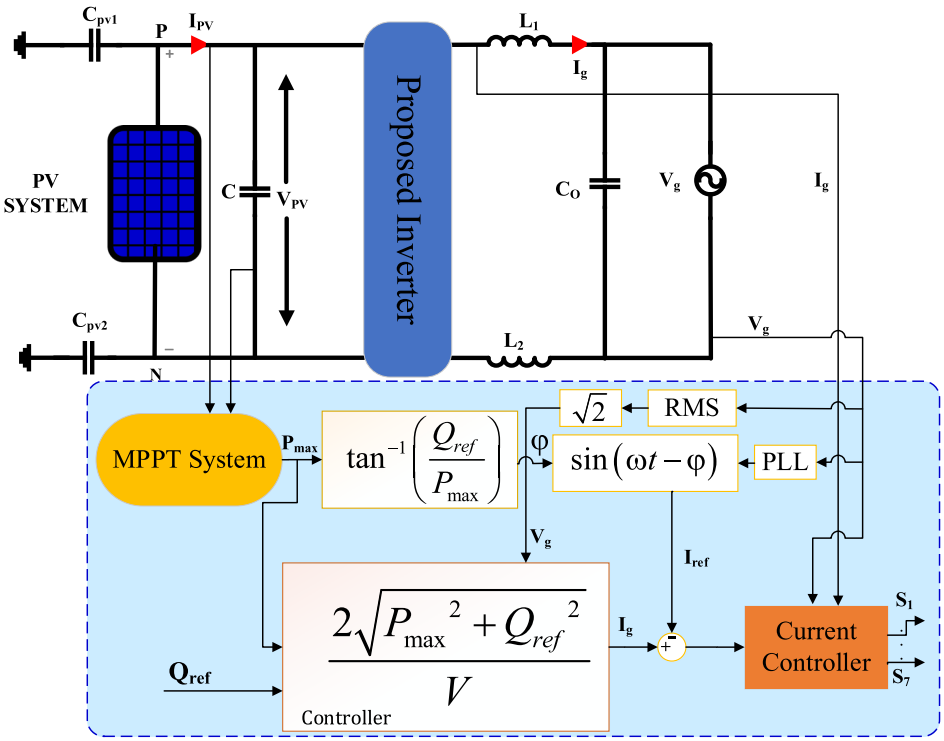


Fig. 11 Control strategy for the proposed transformerless inverter

Fig. 12 Control schematic of grid-connected PV system with proposed inverter



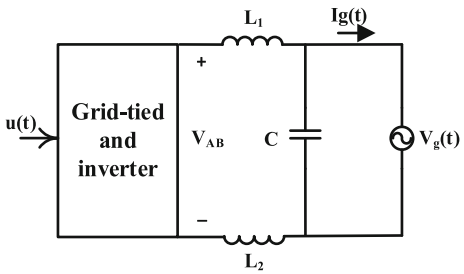


Fig. 13 Equivalent circuit of the system with control input u(t)

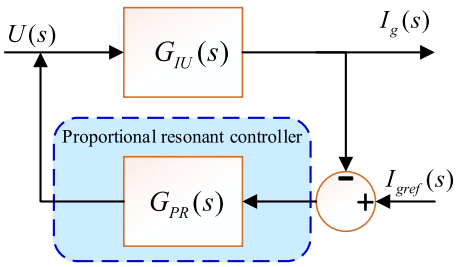


Fig. 14 Block diagram of closed-loop current controller

For voltage control ($PM = 50°$):

$$K_{IV} \leqslant \frac{\omega_{CV} \times K_{PV}}{tan\theta} = \frac{100\pi \times K_{PV}}{1.192} = 105 \times K_{PV} \quad (29)$$

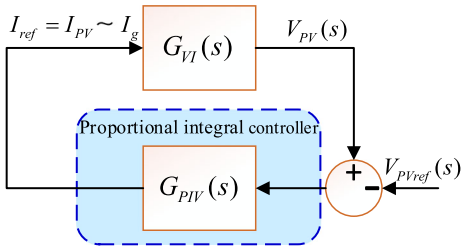


Fig. 15 Block diagram of closed-loop voltage controller

Condition (II)

At the cutoff frequency, the size of the open-loop transfer function is equal to 1 ($G_{OLC}(j\omega_c) = 1$). For current control:

$$\begin{aligned}
&\frac{V_{PV}}{L\omega_c}\left[\sqrt{\frac{(K_P \times \left(\omega_1^2 - \omega_C^2\right)^2)^2 + (2 \times \omega_{PRC} \times \omega_c \times (K_P + K_r))^2}{(\omega_1^2 - \omega_C^2)^2 + (2 \times \omega_{PRC} \times \omega_c)}}\right] \\
&= 1 = \frac{(\omega_1^2 - \omega_C^2)^2}{(\omega_1^2 - \omega_C^2)^2 + (2 \times \omega_{PRC} \times \omega_c)} \times K_P^2 \\
&+ \frac{(2 \times \omega_{PRC} \times \omega_c)^2}{(\omega_1^2 - \omega_C^2)^2 + (2 \times \omega_{PRC} \times \omega_c)} \times (K_P + K_r)^2 \\
&= \left(\frac{L \times \omega_c}{V_{PV}}\right)^2 = \left(\frac{6 \times 10^{-3} \times 2000\pi}{400}\right)^2 \cong 0.094
\end{aligned} \tag{30}$$

For voltage control:

$$\begin{aligned}
K_{IV} &= \sqrt{\left(2 \times C_{pv}\right)^2 \times \omega_{CV}^4 - K_{PV}^2 \times \omega_{CV}^2} \\
&= 100\pi\sqrt{\left(2 \times 1100 \times 10^{-6} \times 100\pi\right)^2 - {K_{PV}}^2} \\
&\cong 100\pi\sqrt{0.4777 - {K_{PV}}^2}
\end{aligned} \tag{31}$$

Condition (III)

The steady-state error must be smaller than a certain limit (steady-state error $\leq \xi$). If $\xi = 0.02$, so

$$(K_P + K_r) \geqslant \frac{L \times \omega_1}{V_{PV}} \times \left(\frac{1}{\xi^2} - 1\right) = (K_P + K_r) \geqslant 11.78 \tag{32}$$

Finally, the controller coefficients are obtained as follows: $K_{PV} = 0.659,\ K_{IV} = 65.9,\ K_p = 0.094,\ K_r \geq 79$

5 Result Analysis and Performance Comparison

In order to assess the performance of the proposed inverter topologies, we conducted a series of simulations using MATLAB/Simulink. The proposed topology was simulated using parameters specified in Tables 3 and 4. The simulation included the implementation of a perturbation and observation (P&O) algorithm to enable maximum power tracking and a voltage controller to stabilize the DC-link voltage. Furthermore, for the proposed topology, proportional resonant (PR) and proportional integral (PI) controllers were utilized. Through these simulations, we were able to thoroughly analyze the performance of both inverter topologies under varying conditions and draw meaningful conclusions about the strengths and limitations of each design.

Table 3 Specification of WHT -305- SunPower SPR

Parameter/specification	Value
Power at maximum power point (P_{MPP})	305 W
Maximum power point voltage (V_{MPP})	54/7 V
Maximum power point current (I_{MPP})	5/58 A
Open-circuit voltage (V_{OC})	64/2 V
Short-circuit current (I_{SC})	5/96 A
Number of cells in series (N_S)	96

Table 4 Inverter specifications

Parameter/specification	Value
Rated power (P)	3.2 kW
DC input voltage	400 V
Grid voltage	1-ph-230 V(RMS)
Grid frequency	50 Hz
Switching frequency	10 kHz
Filter inductors (L)	3 mH
Filter capacitor (C)	6 nF
DC-link capacitors (C_1)	2200 µF
DC-link capacitors (C_2)	2200 µF
Stray capacitors (C_{PV1})	300 nF
Stray capacitors (C_{PV2})	300 nF

5.1 Specifications of the Proposed System

A description of the WHT-305-SunPower SPR photovoltaic module and the specifications of the different parts of the proposed system, including the inverter and network, can be found in Tables 3 and 4.

5.2 Simulation and Experimental Result in Proposed Topology

5.2.1 Simulation Results

In this section, we present the simulation results using MATLAB/Simulink for the three-level inverter. In the simulation,

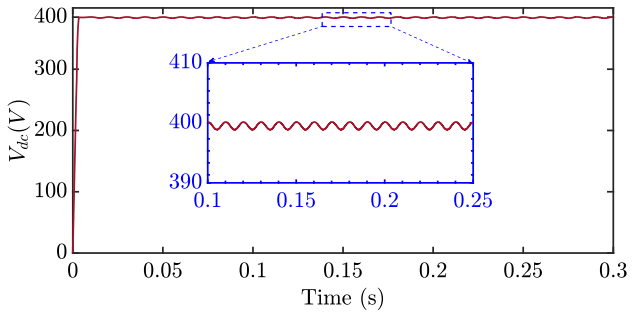


Fig. 16 DC-link voltage output

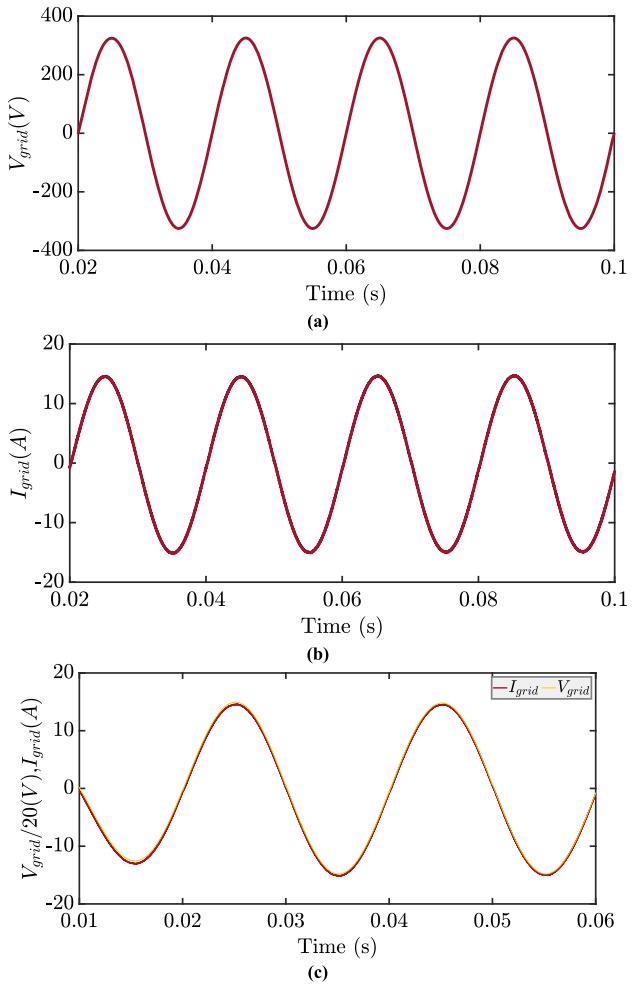


Fig. 17 Grid voltage (**a**), grid current (**b**), grid voltage and current with changing reactive power (**c**)

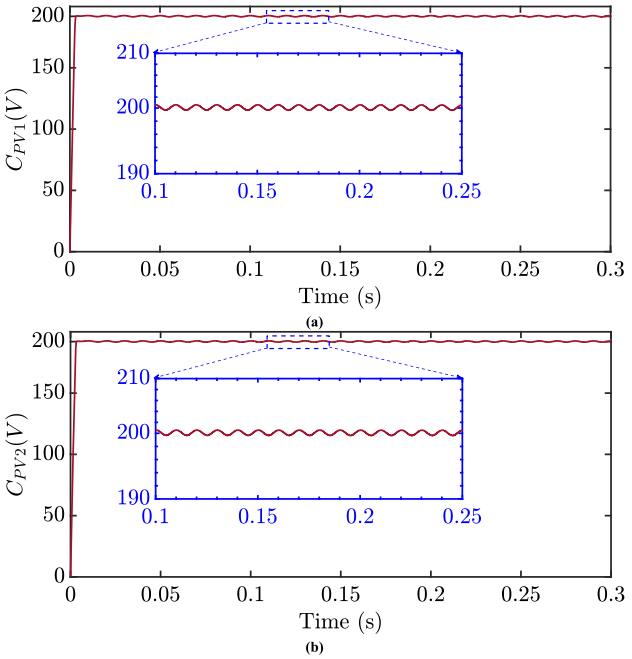


Fig. 18 DC-link capacitors (C_1) (**a**) DC-link capacitors (C_2) (**b**)

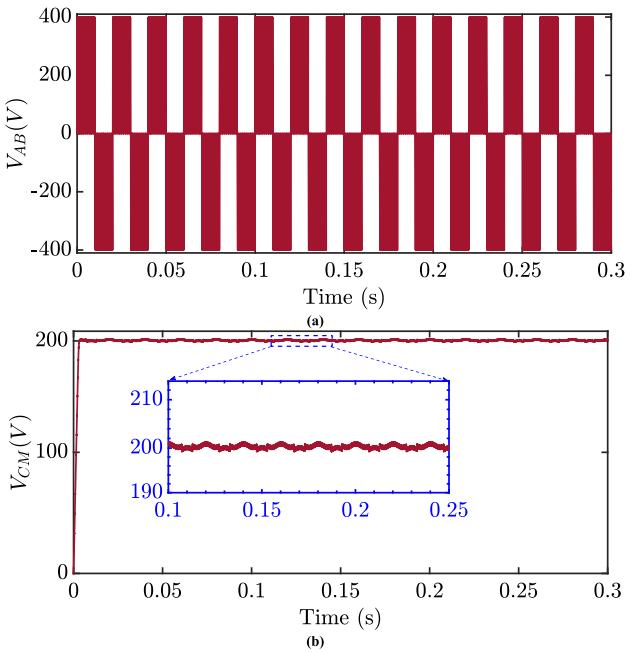


Fig. 19 V_{AB} (**a**)V_{CM} (**b**)

the peak input voltage is set to 400 V_{dc}, as shown in Fig. 16. Additionally, the proposed topology supports grid reactive power. Consequently, Fig. 17a, b and c displays the grid voltage and current, grid-injected current and the output inverter voltage at various reactive powers. The voltage waveforms of capacitors C_{PV1}, C_{PV2} and V_{AB}, V_{CM} are illustrated in Fig. 18a-b and Fig. 19a-b. From these waveforms, it can be observed that the capacitor voltage is regulated to half of the input voltage, and the voltage ripples are within an acceptable range. Figure 20a-b shows the voltage of the A and B points in the proposed inverter with respect to the ground. Figure 21a-b shows the values of the leakage currents through spray capacitors in MATLAB/Simulink. According to these figures, it is clear that the RMS value of the current is 0.001084 mA, and

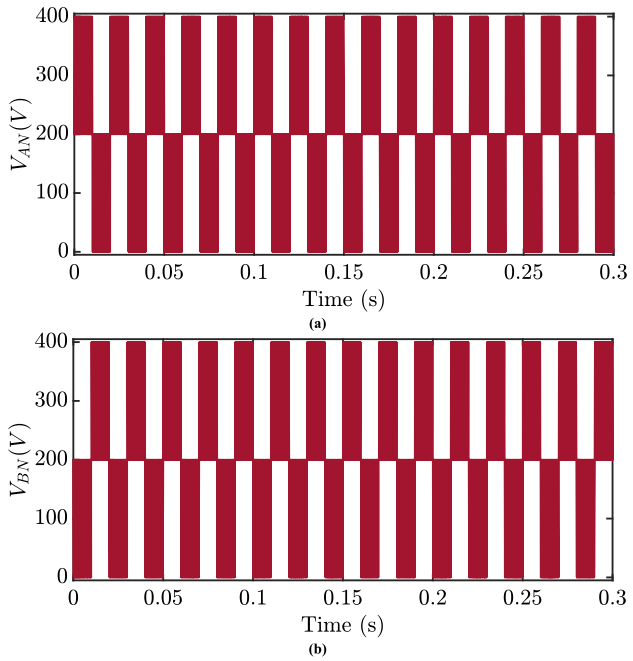


Fig. 20 V_{AN} (**a**) V_{BN} (**b**)

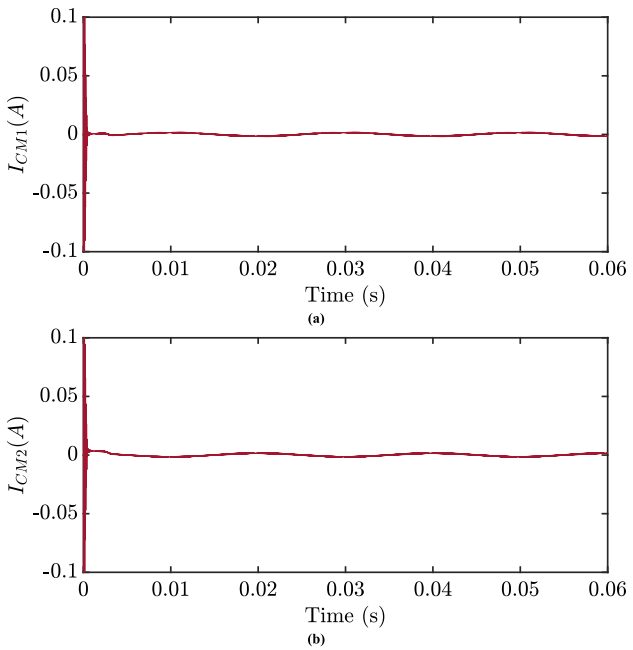


Fig. 21 Leakage capacitor current (C_{PV1}) (**a**) and leakage capacitor current (C_{PV2}) (**b**)

the peak value of the current is 0.001553 mA. In addition, grid current THDs is shown in Fig. 22. Finally, the efficiency value of the proposed inverter is 99.77%, which is extraordinarily high and impressive compared to other proposed inverters. Figure 23 shows this incredible efficiency.

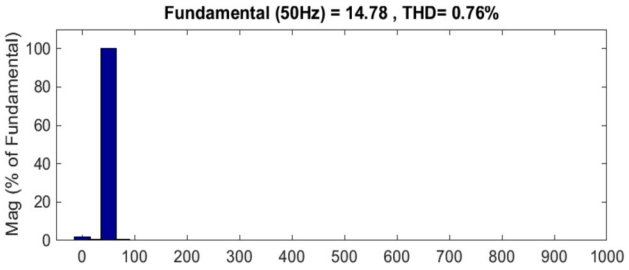


Fig. 22 The spectrum and harmonic distortion of the grid current

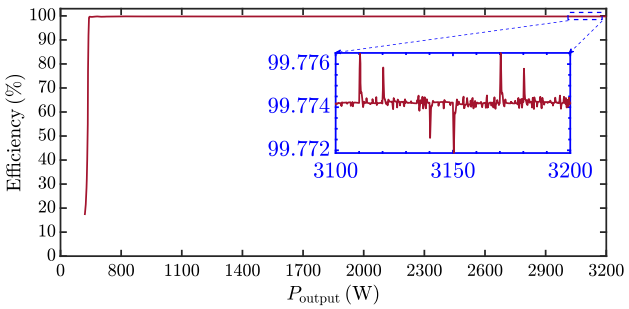


Fig. 23 Efficiency of the proposed topology

5.2.2 Experimental Results

Experimental results are provided to verify the performance of the proposed inverter. Figure 24 shows a photograph of the proposed inverter prototype. The details of the components used, and the proposed inverter specifications are listed in Table 5. Figure 24 shows the laboratory prototype of the single-phase grid-tied proposed inverter used in the experiment. This physical setup includes all necessary components listed in Table 5, configured for testing and validation of the proposed inverter topology.

Figure 25 presents several waveforms captured during the operation of the proposed inverter:

Output Voltage (V_{out}): The peak value of the output voltage is approximately 311 V, which corresponds to an RMS value of 220 V, matching the grid voltage specification.

Output Current (I_{out}): The output current waveform shows a peak value of approximately 13 A, indicating the current delivered to the grid.

Three-Level Output Voltage ($V_{out(3\text{-}level)}$)): The three-level output voltage waveform exhibits distinct levels with peak values of around 400 V, −400 V, and 0 V, demonstrating the effective modulation technique used in the inverter.

Input Voltage (V_{in}): The input voltage remains steady at 400 V, ensuring a consistent power supply to the inverter.

Figure 26 shows the following waveforms:

Output Voltage (V_{out}): The peak value of the output voltage is again around 311 V.

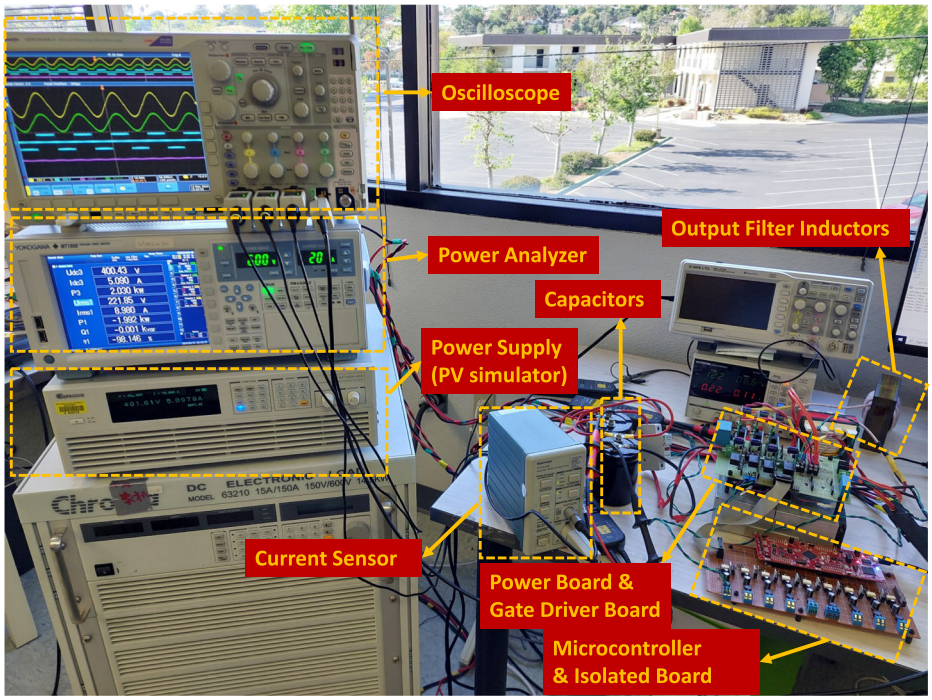


Fig. 24 Laboratory prototype of the single-phase grid-tied proposed inverter used in the experiment

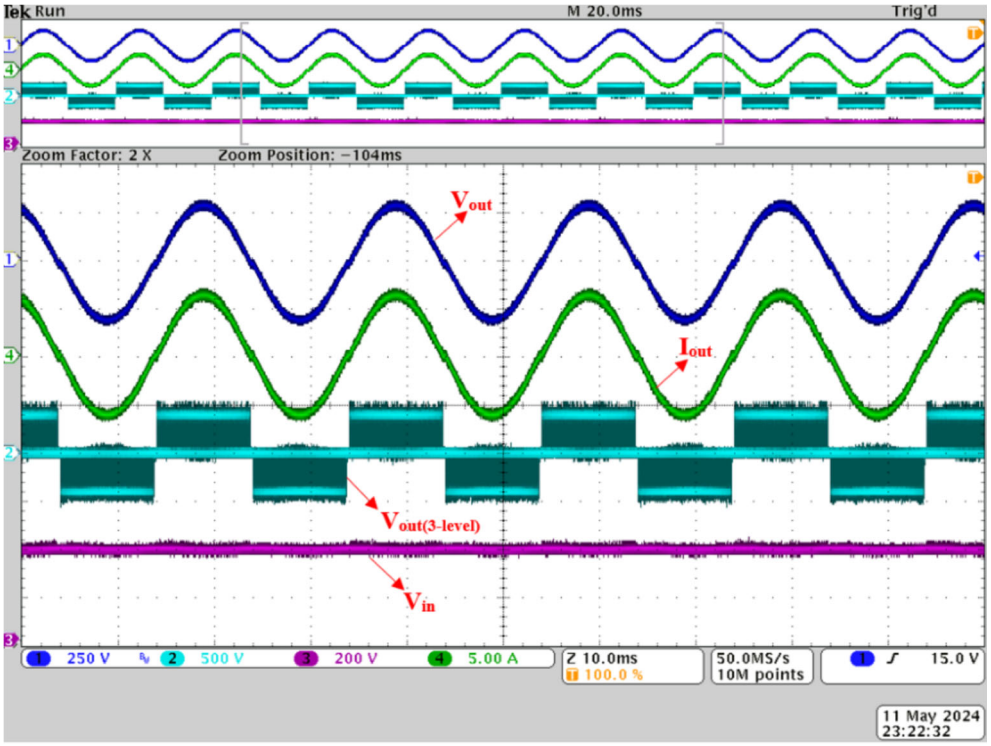


Fig. 25 Output voltage (V_{out}), output current (I_{out}), three-level output voltage ($V_{out(3\text{-}level)}$), input voltage (V_{in}) waves form of proposed inverter

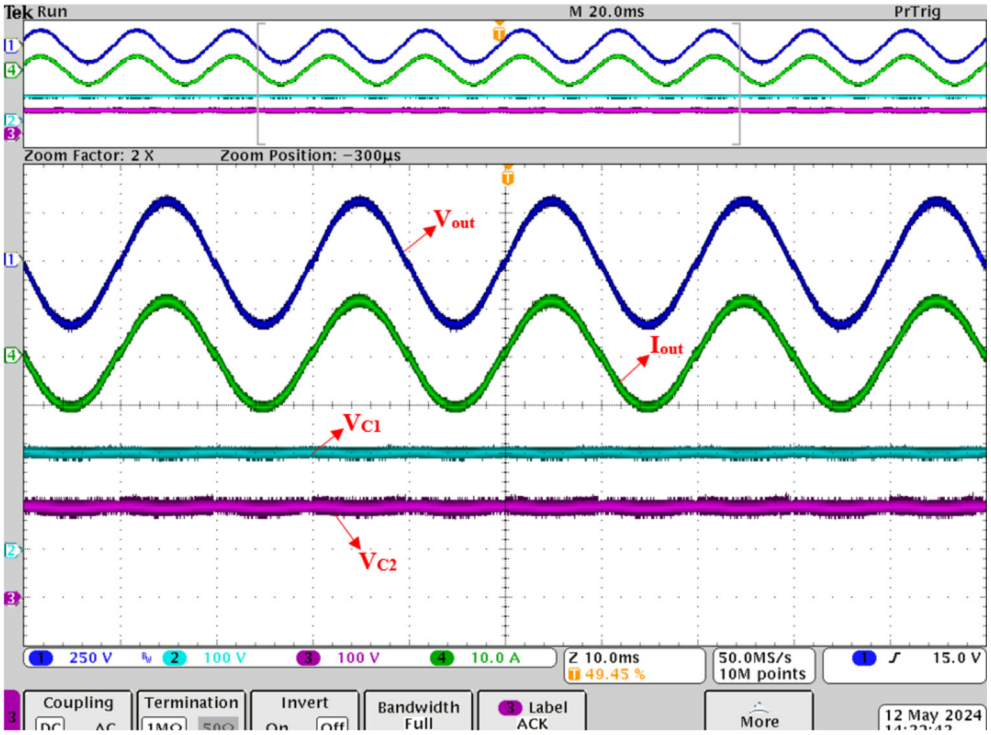


Fig. 26 Output voltage (V_{out}), output current (I_{out}), voltage across capacitors (V_{C1},V_{C2})

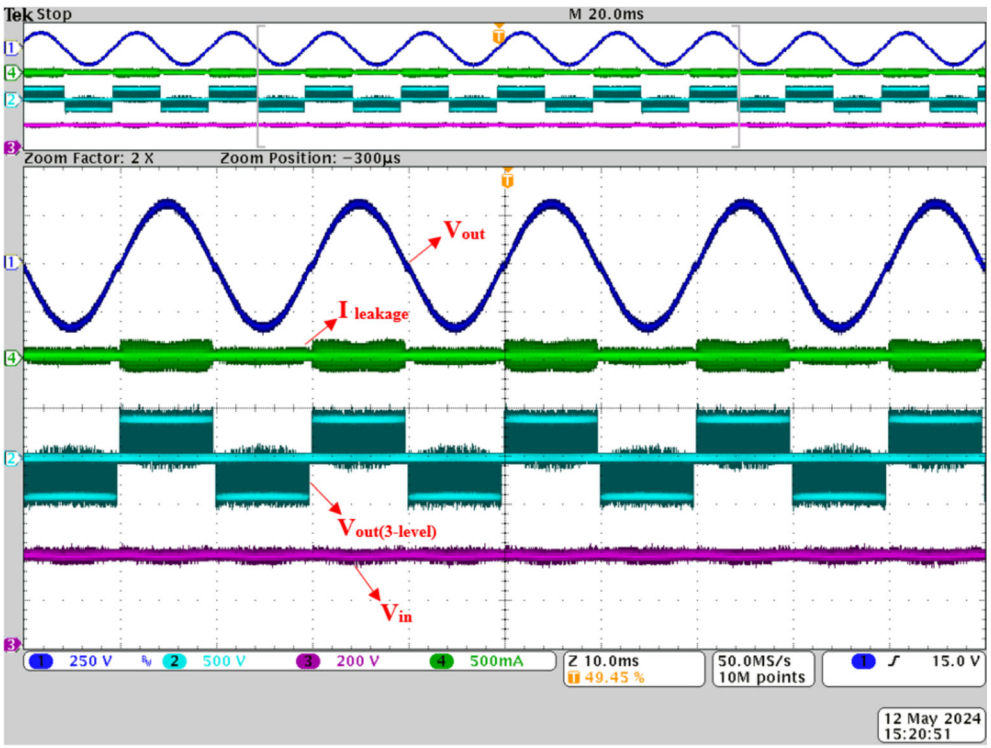


Fig. 27 Output voltage (V_{out}), leakage current ($I_{leakage}$), three-level output voltage ($V_{out(3\text{-}level)}$), input voltage (V_{in}) waves form of proposed inverter

Table 5 Details of utilized components in proposed topology

Parameter/specification	Type	Value
Rated output power		2 kW
DC input voltage		400 V
Grid voltage		1-ph-220 V(RMS)
Grid frequency		50 Hz
Switching frequency		32 kHz
Filter inductors L_f		500 µH
Filter capacitor C_f		1 µF
DC-link capacitors C_1		3300 µF
DC-link capacitors C_2		3300 µF
Parasitic capacitors (C_{PV1})		300 nF
Parasitic capacitors (C_{PV2})		300 nF
Microcontroller	TMS320F280049	
Power switches	C2M0080120D	
Gate driver	ACPL-H342	
Isolated DC–DC converter	MGJ2D121505SC	

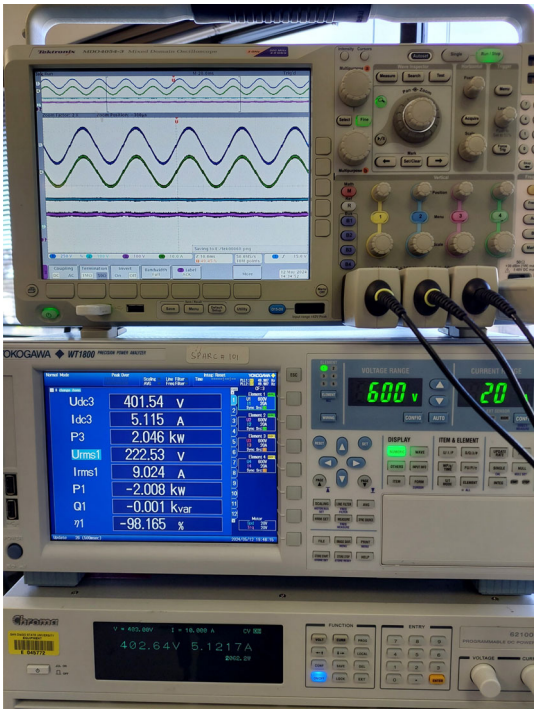


Fig. 29 Experimental results values of proposed single-phase inverter

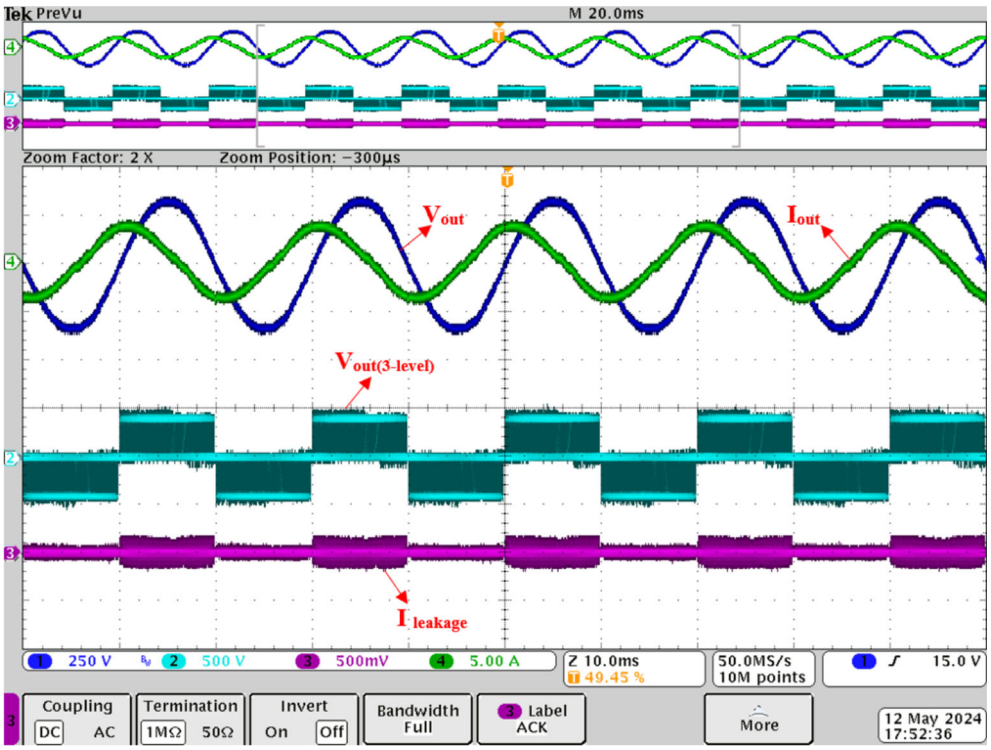


Fig. 28 Output voltage (V_{out}), output current (I_{out}), three-level output voltage ($V_{out(3\text{-}level)}$), leakage current ($I_{leakage}$) waves form of proposed inverter

Table 6 Comparison of different transformerless inverter topologies (NA = Not available in the publication)

Topology name	Semiconductor devices		Leakage current (mA)	Passive filter		Output voltage level	Grid current THD %	Efficiency (simulation) %	Efficiency (experimental) %
	No. of IGBTs	No. of Diodes	RMS	No. of L	No. of C				
Virtual DC Bus [38]	5	0	0.75	1	1	3	5.1	96.8	94.2
Modified H6 [39]	7	0	9.1	0	2	3	2.3	92.18	97.04
H6-III [28]	6	0	9.8	1	2	3	1.1	92.75	97.6
Improved H6 [40]	6	0	10	1	2	3	1.8	NA	NA
2D-H5 [41]	5	2	17	1	2	3	NA	96.8	96.2
Flying Capacitor-II [29]	4	1	0.58	1	1	3	4.2	97.2	99.04
HERIC [42]	6	0	23.2	1	2	3	1.7	95.03	NA
H6(Passive clamped) [43]	6	2	5.1	1	2	3	1.1	NA	97.16
HBZVR-D [44]	5	6	5.4	1	2	3	1.2	92.8	95.3
Improved H6 [45]	6	1	1.1	0	3	3	0.95	NA	98.1
Proposed Topology	7	0	1.084	1	2	3	0.76	99.77	98.16

Output Current (I_{out}): The peak current remains at approximately 13 A.

Voltage Across Capacitors (V_{C1}, V_{C2}): The voltages across capacitors C1 and C2 are shown to have peak values of around 200 V each, indicating balanced voltage distribution and effective DC-link capacitor utilization.

Figure 27 presents waveforms including:

Output Voltage (V_{out}): The output voltage maintains a peak value of 311 V_{dc}.

Leakage Current ($I_{leakage}$): The leakage current waveform shows a peak value of approximately 100 mA, which is very low and within safe operational limits.

Three-Level Output Voltage ($V_{out(3\text{-}level)}$): The three-level voltage output maintains peak values of 400 V, −400 V, and 0 V.

Input Voltage (V_{in}): The input voltage remains at a steady 400 V_{dc}.

Figure 28 shows the performance of the inverter at non-unity power factor load and includes the following waveforms:

Output Voltage (V_{out}): The output voltage shows a peak value of 311 V_{dc}.

Output Current (I_{out}): The output current exhibits a peak value of 4 A.

Three-Level Output Voltage ($V_{out(3\text{-}level)}$): The three-level output voltage maintains peaks at 400 V, −400 V, and 0 V.

Leakage Current ($I_{leakage}$): The leakage current continues to show a peak value of around 100 mA, reaffirming the inverter's design efficacy in minimizing leakage current.

Finally, in order to show the experimental efficiency of the proposed inverter, Fig. 29 is given. In this figure, the image of the oscilloscope is shown along with the power analyzer panel. The input voltage is 400 V, and the DC input current is about 5.11A. Also, the effective value of the output voltage is 222.5 V and the effective value of the output current is 9.02A, which makes the output power about 2 kW. According to this figure, it can be seen that the experimental efficiency of the inverter has been measured at 98.16%, which is a very high efficiency for single-phase inverters. To better understand the performance of the proposed inverter, we have conducted a comprehensive comparison of its leakage current with that of other inverter topologies. Table 6 provides a detailed breakdown of the comparison, including the number of switches, diodes, filter capacitors, filter inductors, and the number of output levels for each topology [36, 37]. This analysis provides valuable insight into the strengths and weaknesses of

different inverter designs and demonstrates the advantages of the proposed topology over other alternatives.

6 Conclusions and Future Works

This paper has presented an innovative transformerless inverter topology for grid-connected photovoltaic systems. The proposed system incorporates the following advancements:

i. The proposed topology reaches a leakage of near zero by carefully examining H5 topology and the use of advanced modulation techniques along with RBIGBT switch.
ii. The inverter can provide reactive power to the grid, resulting in an impressive efficiency of 99.77% in simulation results and 98.16% in experimental results.
iii. The use of a three-level output voltage significantly reduces the total harmonic distortion of the current to only 0.76%.

The viability of the proposed topology has been validated through both simulation and experimental studies. Overall, the novel topology offers a highly efficient and reliable solution for grid-connected photovoltaic systems, with the added benefits of low leakage current and reduced harmonic distortion.

Despite the promising results, there are certain limitations that need to be addressed in future research. One of the main limitations is the increased complexity of the modulation technique, which may pose challenges for practical implementation, especially in low-cost applications. Additionally, the reliance on the RBIGBT switch, while beneficial for leakage current reduction, may lead to increased system costs and component availability concerns in large-scale deployments. Thermal management is another critical aspect that requires further investigation to ensure stable operation under high-load conditions and prolonged operational periods. Moreover, the proposed topology's performance under extreme grid conditions, such as voltage sags and frequency fluctuations, has not been extensively analyzed and requires further exploration to guarantee grid code compliance.

Future research efforts will focus on addressing these challenges by optimizing the control algorithms to simplify the modulation strategy and enhance computational efficiency. Advanced control methods, such as model predictive control and artificial intelligence-based algorithms, will be investigated to improve the dynamic response and adaptive performance of the inverter. Efforts will also be directed toward enhancing the thermal management system through the implementation of innovative cooling solutions and component-level improvements to ensure long-term reliability. Furthermore, scaling the topology for higher power applications and conducting extensive field testing under diverse environmental and grid conditions will provide deeper insights into its real-world applicability. A comprehensive economic feasibility analysis will be conducted to assess the cost-performance trade-offs and determine the suitability of the proposed inverter for widespread commercial deployment.

Finally, the proposed transformerless inverter topology presents a cost-effective, highly efficient, and reliable solution for grid-connected PV systems, offering significant improvements in leakage current suppression, power quality, and overall system efficiency. However, addressing the identified limitations and focusing on future enhancements will be crucial for ensuring the practical viability and broader adoption of the proposed design in modern photovoltaic power generation systems.

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Data availability Data will be made available on request.

Declarations

Conflict of interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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