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Single Ended Read Decoupled High Stable 9T CNTFET SRAM for Low Power Applications

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ABSTRACT

In wireless sensor networks, conserving power is vital for prolonging battery life. This research introduces a groundbreaking solution: a 9T carbon nanotube-field effect transistor (CNTFET) based SRAM cell (9T SRAM) designed to optimize power consumption and stability. Through meticulous analysis, the performance of this 9T SRAM cell is quantified. Power consumption metrics reveal impressive figures: the write, hold, read, and dynamic power are measured at 0.21 nW, 0.32 nW, 15.28 μW, and 8.09 μW, respectively. Furthermore, the Write SNM (WSNM), Hold SNM (HSNM), and Read SNM (RSNM) are found to be 380.11, 390.22, and 390.31 mV, respectively, indicating robust stability. The proposed bit cell has a write and read delay of 95.1 and 39.6 pS, respectively. Incorporating stacked transistors diminishes power consumption, while the decoupled read technique boosts the stability of the proposed bit cell. By comparing these results with existing SRAM cells, the superiority of the proposed 9T SRAM cell in terms of power efficiency becomes evident. Notably, it outperforms earlier models, making it an ideal candidate for integration into wireless sensor networks. These findings are supported by simulations conducted using HSPICE, alongside a 32 nm CNTFET model sourced from Stanford University.

1 | Introduction

1.1 | Motivation

The metal oxide semiconductor field-effect transistor (MOSFET) stands as a foundation in VLSI architecture, serving as a fundamental building block for electronic systems and circuits. Its widespread use is attributed to several distinct advantages, including lower power consumption, enhanced speed, compactness, and high input impedance [1]. However, as technology scales down, MOS devices face challenges such as increasing leakage power consumption, gate control degradation, short-channel effects, and process variation, rendering them less suitable for nano-scale circuit design. To address these limitations and meet the demands of nano-scale VLSI design, researchers are actively seeking alternatives to the MOSFET [2]. In line with the International Technology Roadmap for Semiconductors (ITRS), the CNTFET emerges as a promising candidate. CNTFET holds the potential to overcome the constraints of MOS devices, offering a pathway to improved performance and efficiency at the nano-scale level [2]. Recognizing the benefits of CNTFET technology, this research adopts it as the fundamental component for the CNFET-based proposed 9T SRAM.

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1.2 | CNT and CNTFET Review

The process of creating a carbon nanotube (CNT) involves rolling up a graphene sheet with a honeycomb structure (Figure 1) into a cylindrical shape. Different arrangements of CNTs are classified as zigzag, armchair, and chiral, corresponding to specific parameters named chiral vectors (m, n) [4]. The chiral vectors also determine the electrical properties of the CNT, influencing its behavior as either a conductor or a semiconductor. When $m=n$ or $|m-n|=3i$ (where i is an integer), the CNT behaves as a conductor; otherwise, it behaves as a semiconductor [4]. CNTFETs utilize CNTs as the channel material, with two main types: single-wall CNTs (SWCNTs), which contain only one CNT in the channel, and multi-wall CNTs (MWCNTs), which have multiple CNTs rolled up along the same axis (Figure 2) [5]. The cross-sectional structure of a CNTFET depicted in Figure 3, shows that the channel consists of three CNTs, forming the core of the device [6]. CNTFETs exhibit unique electrical characteristics, including ballistic transport, high transconductance, a high ON/OFF current ratio, low leakage current, and high speed. Despite these attributes, the working principle of CNTFETs aligns with that of MOSFETs [7]. Moreover, CNTFETs demonstrate robustness against process variation, with minimal impact on Vth even with significant temperature variations (from 27°C to 227°C), varies the Vth of CNTFET by only 4.6% [5].

The width of CNTFET (W_{CNTFET}) is determined by [8]:

$$W_{\mathrm{CNTFET}} = (N-1)S + D_{\mathrm{CNT}} \tag{1}$$

where, N-number of CNT, S-pitch value (Spacing between the adjacent CNTs). The chiral vectors, threshold voltage of CNTFET (V_{th}), and D_{CNT} depend on each other as given below [8].

$$D_{CNT} = \frac{a\sqrt{n^2+nm+m^2}}{\pi} \tag{2}$$

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{qD_{CNT}} \tag{3}$$

where, a, V_π, and q refer to atomic distance between carbon atoms, carbon bond energy ($V_\pi = 3.033$ eV) and electronic charge respectively [8].

The current through the drain terminal of CNTFET (I_{DS}) is given by [3]:

$$I_{DS} = \frac{qkT}{\pi h}\left\{ ln\left[1+e^{\frac{\Delta E_F + q\left(\Psi_{cnt(0)}\right) - V_{ss} - \Phi_0 - E_C}{KT}}\right] - ln\left[1+e^{\frac{\Delta E_F + q\left(\Psi_{cnt(L)}\right) - V_{ds} - \Phi_0 - E_C}{KT}}\right]\right\} \tag{4}$$

$$\Delta E_F = kTln\left(1+\frac{n}{\left(\frac{8kT}{\pi V_\pi a\sqrt{3}}\right)\left(\frac{1}{\sqrt{kT}}\int_0^{\frac{6E_C}{T}}\left(\frac{kTx+E_C}{\sqrt{x(kTx+2E_C}}\exp(-x)dx\right)\left(\exp\left(\frac{-E_C}{kT}\right)\right)\right)}\right) \tag{5}$$

Where, h-Planck's constant, ΔE_F-fermi level shift due to doping effect, n-doping concentration, k-Boltzmann constant, T-temperature, E_C-conduction band energy, Ψ_{cnt}-CNT's front gate surface potential, and Φ_0-CNT's back gate surface potentials [3].

1.3 | Discussion on Various SRAM Designs

Research on CNTFET SRAM is crucial due to its significant impact on VLSI systems, occupying 80% of the die size and consuming 70% of the total power [1]. SNM (Static Noise Margin) and power efficiency are critical metrics for SRAM cells, particularly affected by MOS device downsizing, which reduces SNM and increases power leakage [9]. Several strategies have been used to create a CNTFET SRAM cell with low power consumption and high stability. Let's delve into the research conducted thus far to enhance the performance of memory cells by modifying the fundamental 6T SRAM cell. The basic 6T SRAM cell features a single read/write path, resulting reduction in the RSNM of the bit cell [10]. By configuring dissimilar read and write paths, we obtain a conventional 8T SRAM cell structure, which enhances the RSNM compared to a 6T SRAM memory cell. However, the operational aspects (write/hold) of both traditional 6T and 8T cells remain the same. Consequently, the

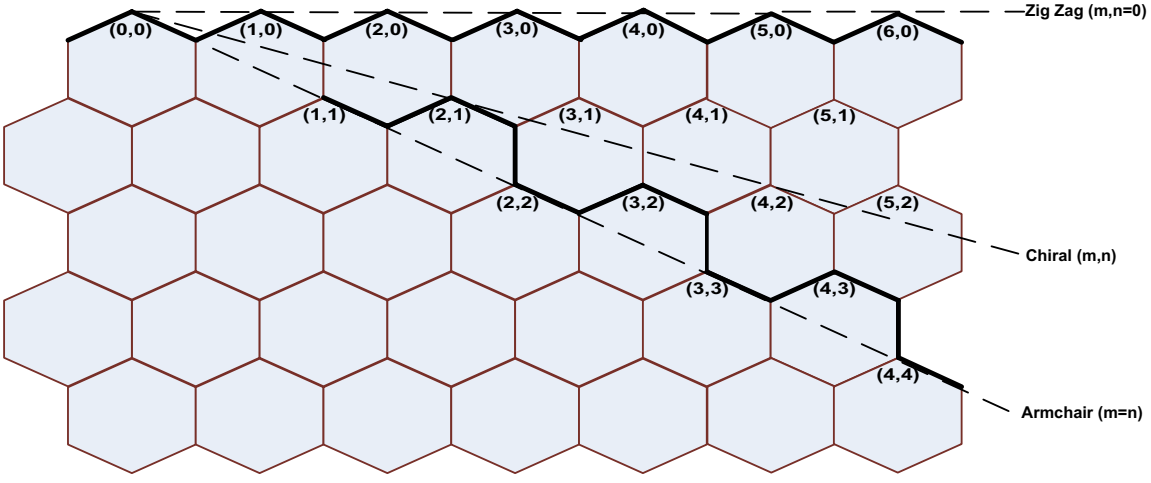

FIGURE 1 | Graphene sheet honey-comb structure (armchair, zigzag and chiral CNT) [3].

power dissipation during write and hold operations is identical for these two cell configurations [8, 11]. To enhance the performance of SRAM cells, researchers have explored configurations employing 9–10 transistors. A notable example is the 10T-P1-3 bit cell, which offers significant advantages over conventional 10T SRAM configurations. This cell consumes 19.8% less access energy per operation and occupies 19.5% less space. Moreover, its RSNM has been improved by approximately 100 mV, making it an optimal choice for low-power sensors and battery-assisted circuits [12]. The 10T single-ended PPN cell features a pull-up network composed of stacked P-MOSFETs. This configuration leads to an increase in RSNM and a reduction in leakage power dissipation. Consequently, the 10T SRAM cell with a single-ended PPN configuration is suitable for deployment in low-power nodes within wireless sensor networks [13]. The TG9T SRAM cell employs read decoupling to achieve high RSNM. The WSNM of the bit cell is improved by utilizing a feedback-cutting method. Additionally, dynamic power consumption can be reduced by minimizing the switching factor of the bit line. Furthermore, the transistor stacking method is utilized to decrease leakage power consumption [14]. The SRAM cell with a bit-interleaving-based bit-line configuration offers low power consumption and rapid access. It boasts features such as high WSNM, low leakage power, and a high (ION/IOFF) ratio. Additionally, the implementation of the read decoupling technique enhances the read stability of the bit cell [15]. The optimized 9T SRAM configuration incorporates stacked P-MOSFETs in its pull-up path. Remarkably, this configuration consumes 58% less power compared to a typical 6T memory cell. Furthermore, the SINM and SVNM of the 9T SRAM cell have been significantly enhanced by 93% and 45%, respectively, compared to the sub-threshold 10T SRAM cell [16]. Various configurations of 9T SRAM cells are compared, with their performance metrics tabulated for analysis. Notably, the incorporation of feedback in the 9T SRAM cell results in reduced write delay and write power [17]. In the pull-down path of the 9T SRAM cell, a sleep transistor is connected, while the pull-up network features stacks of transistors. This configuration effectively reduces the SRAM cell's leakage power consumption compared to an 8T SRAM cell [18]. In the 9T SRAM cell, both static and leakage power are significantly lower compared to the 6T configuration, primarily attributed to the integration of a sleep transistor [19]. Additionally, the SNM in the 9T SRAM cell is 18.9% greater than that of the 6T counterpart [20]. The single-bit-line 9T SRAM cell demonstrates lower power consumption compared to dual-bit line structures, where both bit lines are precharged during read/write operations. Precharging a single-bit line proves to be sufficient in the 9T SRAM cell for read/write operations. Consequently, the single bit-line 9T SRAM memory cell requires less power than traditional structures. Moreover, in comparison to conventional cells, the single bit-line 9T SRAM cell exhibits a higher RSNM [21]. A 32 kb 9T SRAM cell employs a bit line read scheme that increases the RSNM of the SRAM cell, surpassing that of the conventional 8T SRAM cell [22]. The performance of SRAM cells constructed using both CNTFET and FINFET devices surpasses expectations, demonstrating advancements not only at the device level but also through circuit-level optimization. Research articles cited below provide evidence of the enhanced performance of memory cells. For instance, in the FinFET-based ST13T SRAM cell, power gating or sleep transistor methodology is implemented, resulting in a remarkable 93% improvement in power

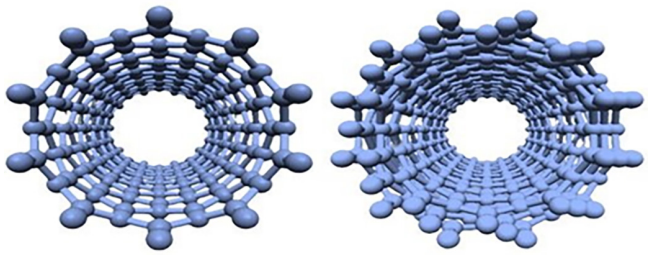

FIGURE 2 | SWCNT tube and MWCNT tube structure [3]. (a) SWCNT (b) MWCNT.

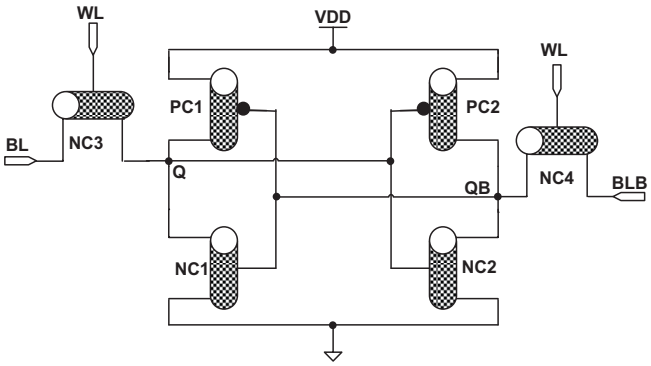

FIGURE 4 | 6T SRAM [8].

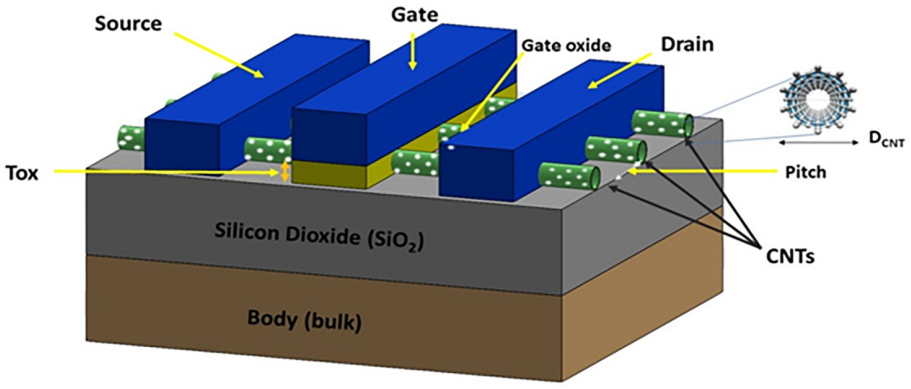

FIGURE 3 | CNTFET structure [3].

consumption. Additionally, utilizing a transmission gate reduces the cell's delay by 12.84% [23]. In an 8T memory cell, the pull-up and pull-down networks are formed by P-type CNTFET and N-type CNTFET, respectively. The addition of transistors in a stacked configuration reduces the cell's power consumption and improves stability during both write and hold modes [10]. The structure of a 10T SRAM cell is derived from adding a separate path to the 8T SRAM cell. This configuration enhances various parameters such as WSNM, HSNM, and RSNM compared to the basic 10T SRAM cell. These improvements are attributed to the cell's dedicated read route topology and stacked transistors [24]. The structures of conventional 6T and 8T CNTFET SRAM memory cells are depicted in Figures 4 and 5, respectively.

1.4 | Key Highlights of the Proposed Work

The 9T SRAM cell introduced in this study achieves commendable performance in terms of stability and power consumption through several key features:

1. Separate read/write operations on distinct bit lines, effectively reducing the bit line's switching activity factor to less than half its value, thereby minimizing dynamic power consumption.
2. Utilization of transistor stacking in the pull-down network of the bit cell leads to a reduction in leakage power dissipation.

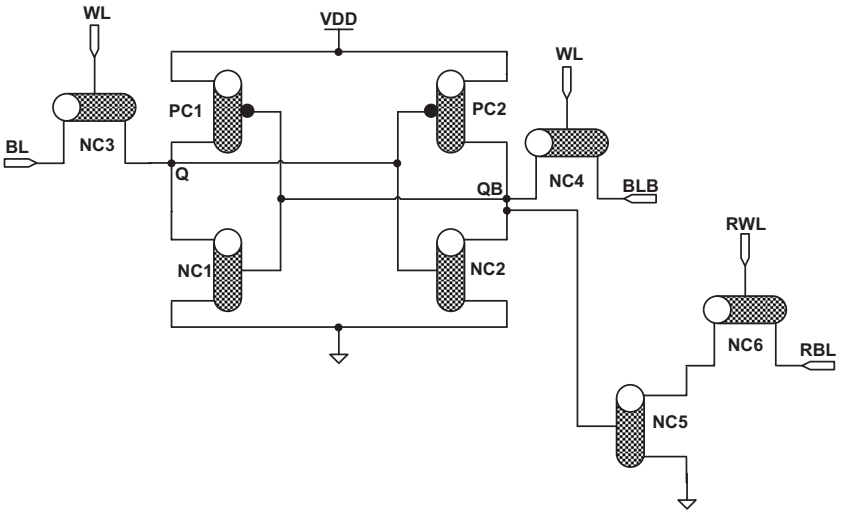

FIGURE 5 | 8T SRAM [12].

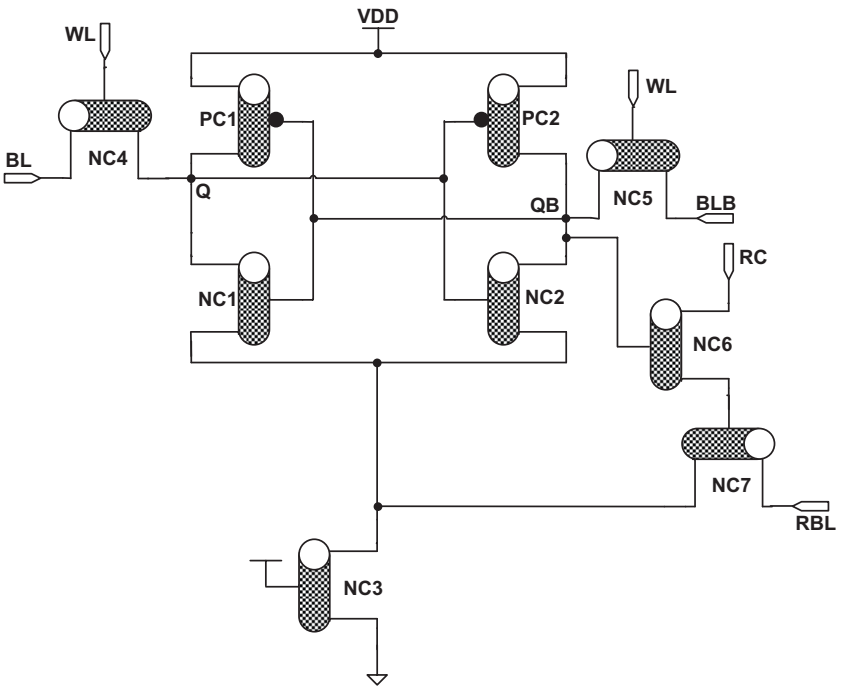

FIGURE 6 | Proposed 9T SRAM cell.

3. Enhancement of RSNM by completely isolating the storage nodes of the core from the read bit line during its read mode.
4. Improved write/hold stability facilitated by the incorporation of stacked transistors.

1.5 | Organization of the Work

The article is structured as follows:

In Section 2, the construction of the proposed 9T SRAM memory cell, utilizing CNTFET technology, is presented. This section covers the structure, functionality, and timing diagram of the proposed cell. Section 3 discusses the findings of the proposed cell and includes a comparison with various other SRAM cells. Finally, Section 4 provides the conclusion of the article.

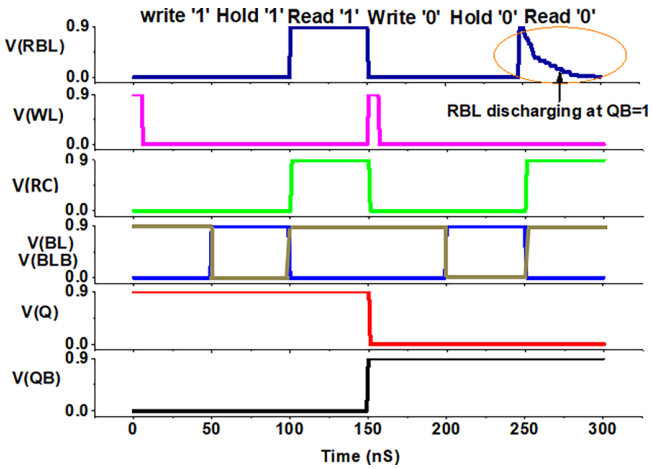

FIGURE 7 | Timing diagram of proposed 9T SRAM cell.

2 | Proposed 9T SRAM Cell Structure and Operation

The proposed memory cell structure comprises nine CNTFETs, forming the core of the SRAM. Specifically, it includes five CNTFETs labeled NC1, NC2, NC3, PC1, and PC2. This memory cell utilizes Q and QB as internal nodes for data storage, accessed via access transistors NC4 and NC5. The gates of NC4 and NC5 are connected to a word line (WL), regulating their switching behavior to store data from the BL and BLB lines into the storage nodes. For reading the memory cell, a dedicated read path is employed, consisting of NC3, NC6, and NC7 CNTFETs. This read path is controlled by read control (RC) and read-bit line (RBL) signals. The circuit diagram of the proposed 9T SRAM memory cell is illustrated in Figure 6, while its timing diagram can be referenced in Figure 7.

2.1 | Write Operation

Figure 8 illustrates the write activity of the storage cell when writing a "1." When the signal values for writing "1" in Q and its complemented value in QB are BL = 1, BLB = 0, and WL = 1, the access transistors NC4 and NC5 are activated. This enables the transfer of BL and BLB values to Q and QB, respectively. Consequently, the data stored in the memory cell is updated to "1" and its complement. This activation turns ON PC1 and NC2, while deactivating PC2 and NC1. As a result, Q is charged to the VDD potential through PC1, and QB is discharged to the ground potential (GND) through NC2 and NC3. This configuration displays bit "1" and "0" at nodes Q and QB, respectively. By maintaining RBL and RC at ground voltage during writing, the

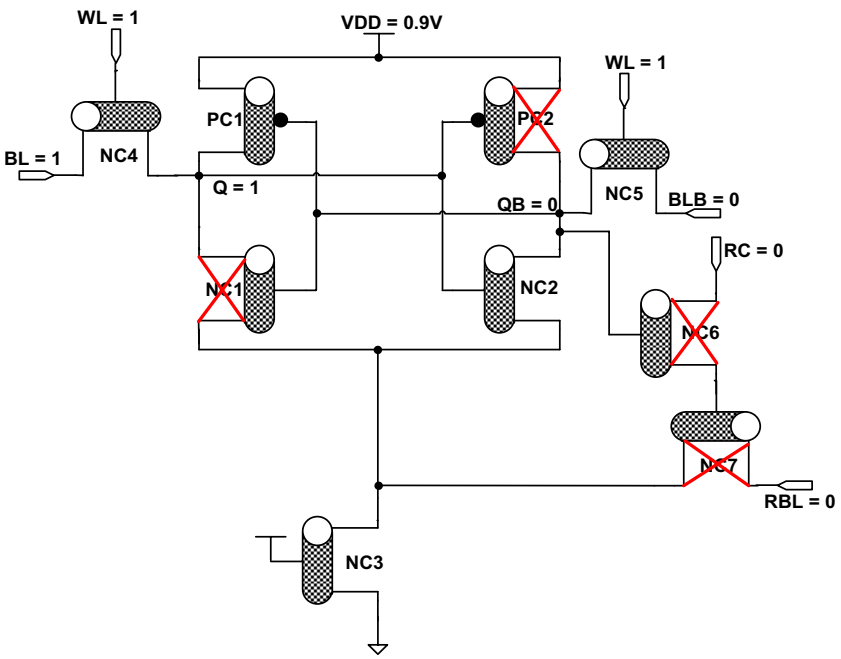

FIGURE 8 | Proposed 9T SRAM cell (write "1" mode).

memory cell is isolated from the read path, ensuring reliable and accurate data writing.

2.2 | Read Operation

Figure 9 depicts the read action of the suggested bit cell when reading a "1." During the read mode, BL, BLB, and WL are held low, while RC and RBL are precharged to VDD. The gate of NC6 is connected to QB. Consequently, when Q = 1 and QB = 0, NC6 and NC7 are in the "OFF" state. Therefore, RBL remains at the precharged potential of VDD. Hence, it can be inferred that the bit cell contains a bit "1" at Q if RBL is maintained at VDD.

To read a "0," the read criteria RC = RBL = 1 are also followed. When Q = 0 and QB = 1, NC6 is activated. Consequently, the gate of NC7 receives the bit "1," enabling NC7 for RC = 1. Subsequently, NC7 and NC3 discharge RBL to ground potential. This signifies that a bit "0" is stored in the bit cell, as observed by the discharge of RBL. Figure 10 illustrates the read "0" operation of the suggested 9T SRAM cell.

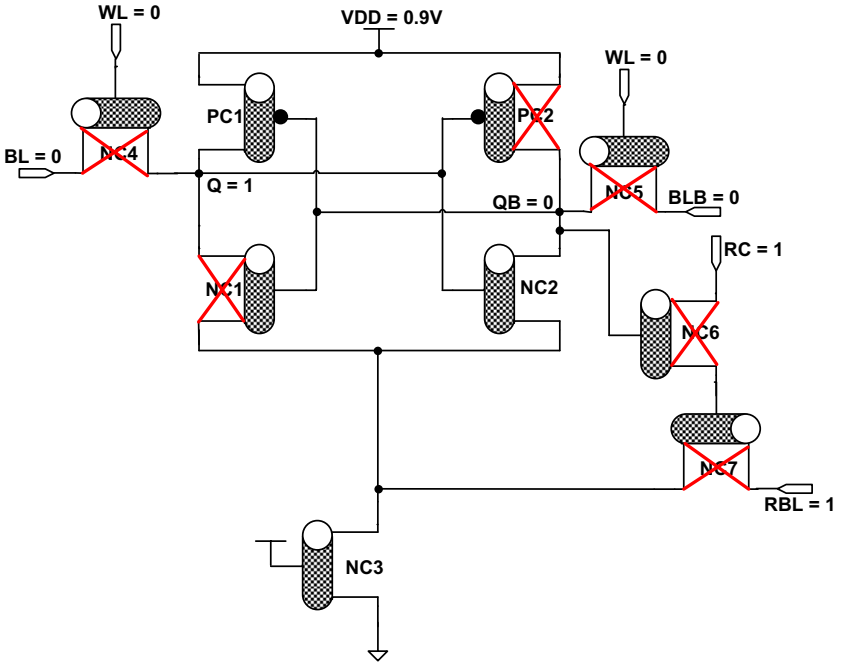

FIGURE 9 | Proposed 9T SRAM cell (read "1" mode).

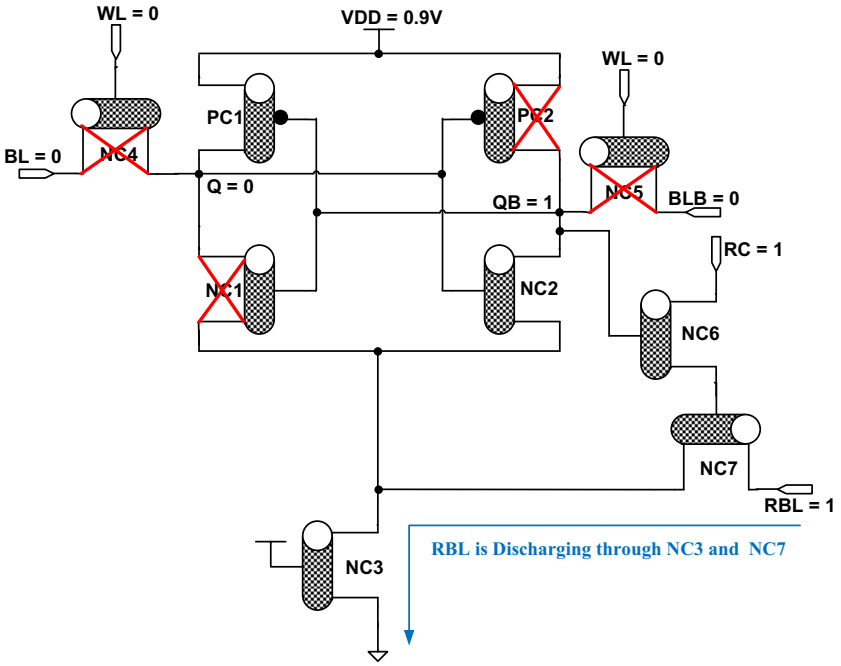

FIGURE 10 | Proposed 9T SRAM cell (read "0" mode).

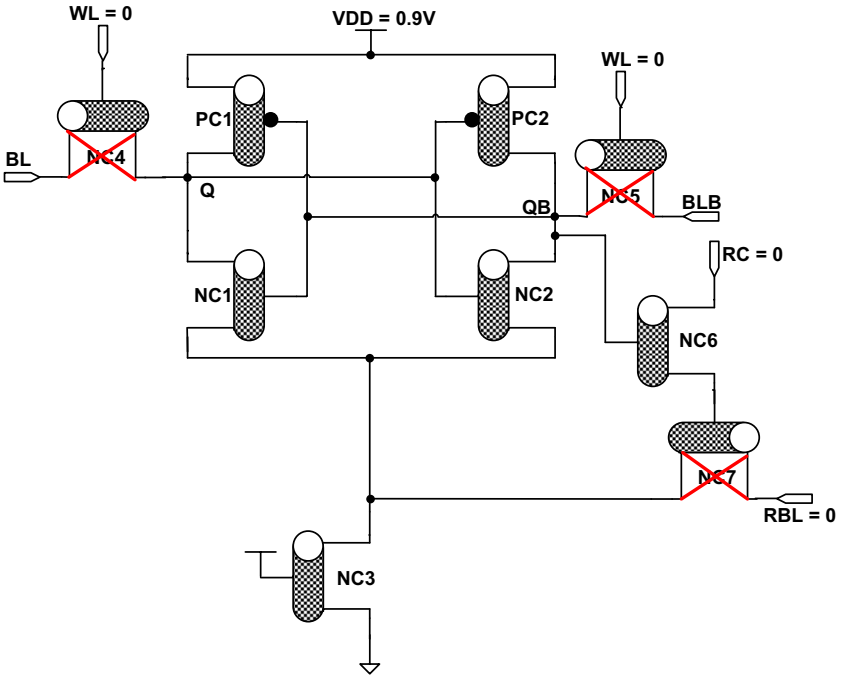

FIGURE 11 | Proposed 9T SRAM cell (hold mode).

TABLE 1 | Signals applied for the operations of proposed 9T SRAM memory.

Signal line	Write "0"	Write "1"	Hold	Read
BL	GND	VDD	—	GND
BLB	VDD	GND	—	GND
WL	VDD	VDD	GND	GND
RBL	GND	GND	GND	Precharged to VDD
RC	GND	GND	GND	VDD

Abbreviations: GND, logic low; VDD, logic high.

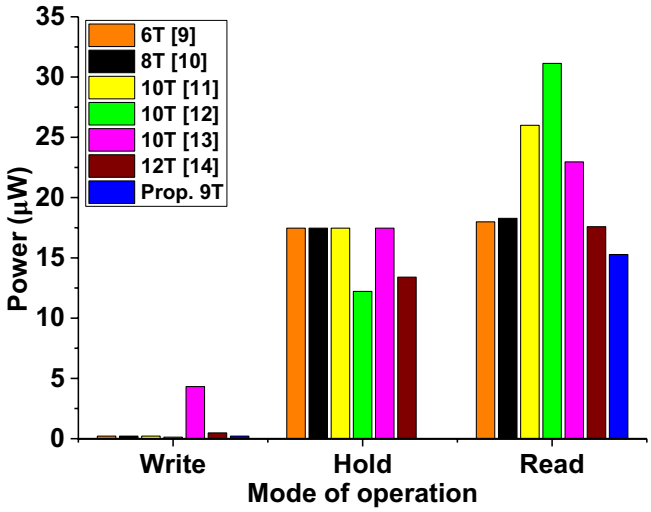

FIGURE 12 | Power consumed by different SRAM cells.

2.3 | Hold Operation

The hold mode is also referred to as standby mode. During the hold operation, the WL, BL, BLB, RC, and RBL are set to ground potential. This action, illustrated in Figure 11, effectively disables transistors NC4, NC5, NC6, and NC7. In the proposed 9T SRAM cell, the storage nodes Q and QB are isolated from the bit lines BL and BLB, respectively, when access transistors NC4 and NC5 are turned OFF. Thus, the suggested cell retains the stored data.

3 | Proposed 9T SRAM Cell's Performance and Analyses

The investigation analyses and compares the performance of the proposed 9T SRAM cell with that of several existing SRAM cells, namely the 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16] SRAM cells that are implemented with CNTFET. Simulation results demonstrate that the power dissipation of the proposed 9T SRAM cell is notably lower than that of all other cells considered, during both hold and read operations. Moreover, the suggested cell surpasses other memory cells regarding write, hold, and read noise margins. In the proposed 9T SRAM memory cell, the presence of NC3 between the ground terminal and the source terminals of NC1 and NC2 transistors causes a shift in the potential of NC1 and NC2 sources above zero voltage. Consequently, the proposed 9T SRAM cell requires higher DC noise to alter the values in nodes Q and QB. This characteristic enhances the SNM of the proposed cell. Additionally, during the reading mode, the RBL is discharged through stacked transistors NC7 and NC3. This configuration reduces the required power in the proposed bit cell during read operation while enhancing its read stability through a separate read path approach. The signals applied for the operations of the proposed 9T SRAM cell are summarized in Table 1.

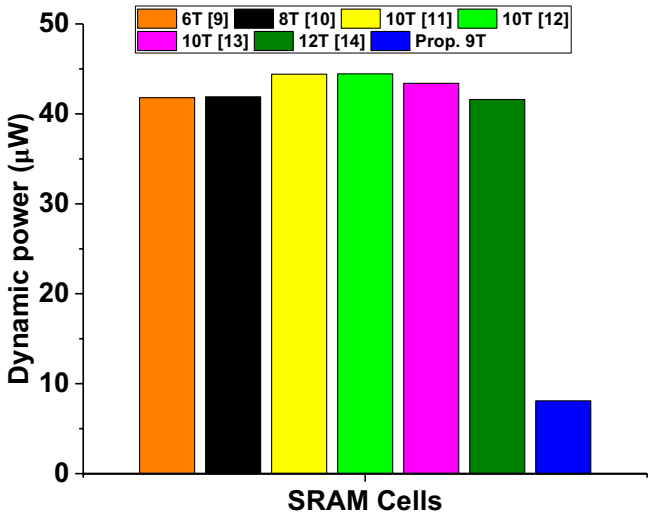

FIGURE 13 | Comparison of dynamic power among various SRAM cells.

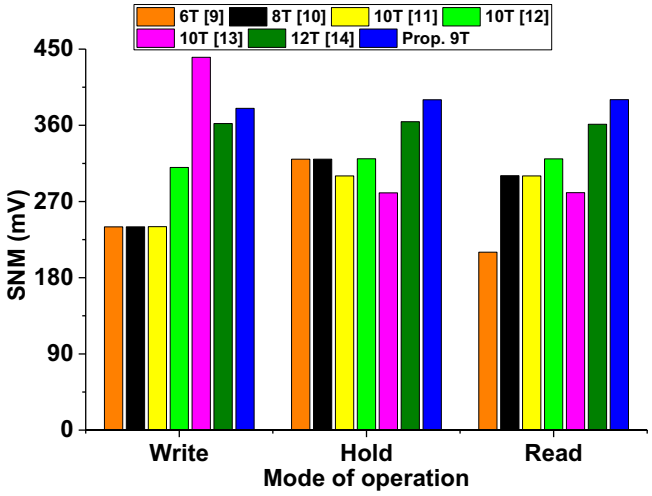

FIGURE 14 | SNM performance of various SRAM cells.

3.1 | Comparison of Various CNTFET SRAM Cells

3.1.1 | Power Analysis

The proposed 9T SRAM memory cell exhibits the following power characteristics: the write, hold, read, and dynamic power dissipation are 0.214 nW, 0.328 nW, 15.28 μW, and 8.09 μW, respectively. In this study, we compare the power consumption of the proposed bit cell with 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16] SRAM cells. Regarding write power dissipation, the suggested 9T cell demonstrates a substantial improvement, with reductions of 95% and 55% compared to 10T [15] and 12T [16] SRAM cells, respectively. During read operation, the power consumed by the proposed cell is notably lower, with reductions of 15%, 16.4%, 41.2%, 50.9%, 33.5%, and 13.1% compared to 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16] SRAM cells, respectively. A detailed comparison of the power characteristics among different CNTFET SRAM cells is visualized in Figure 12.

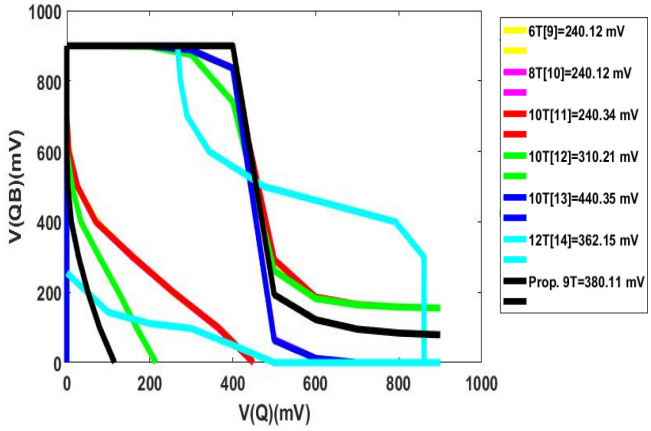

FIGURE 15 | Write SNM butterfly curve of different SRAM cells.

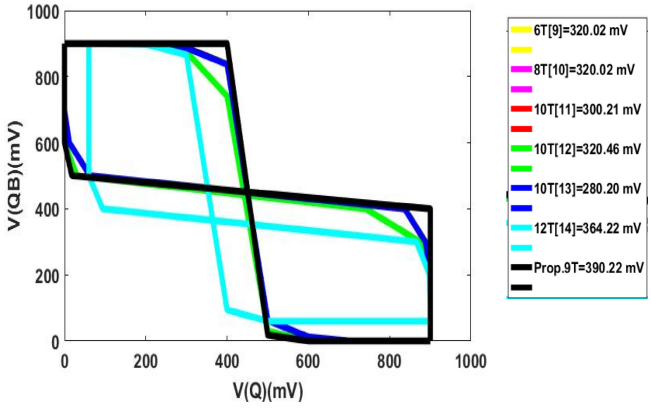

FIGURE 16 | Hold SNM butterfly curve of different SRAM cells.

The dynamic power consumption of a memory cell due to transistor switching activities is determined by various factors including operating frequency (f), effective capacitance or load capacitance (C_L), VDD, and switching factor (α). This power dissipation can be mathematically expressed as [19]:

$$P_{\text{Dynamic}} = \alpha \times C_L \times f \times \text{VDD}^2 \tag{6}$$

Therefore, the dynamic power consumption of an SRAM cell is influenced by the charging and discharging of bit lines and control signals associated with the bit cell [15]. In the proposed cell, the dynamic power is significantly lower compared to other configurations. Specifically, it is 80.6%, 80.6%, 81.8%, 81.8%, 81.4%, and 80.6% lower than 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16] SRAM cells, respectively. For a comprehensive comparison, the dynamic power consumption of different SRAM cells has been calculated and illustrated in Figure 13.

3.1.2 | Stability Analysis

The SNM assesses the endurance of a memory cell under working conditions. It represents the maximum DC noise voltage that an SRAM cell can sustain without changing its state while it is in use. Noise voltage is applied to the storage nodes in order to analyze the voltage transfer characteristics (VTC) of the

inverters. The VTC curves of the two inverters are combined to create a butterfly curve. Inside the smallest lobe of the butterfly curve, fix the largest square. The bit cell's SNM and the square's length are equal [3].

The WSNM of the proposed cell is significantly higher compared to other SRAM configurations. Specifically, it is 1.58×/1.58×/1.58×/1.22×/1.04× times higher than 6T [8], 8T [12], 10T [13], 10T [14], and 12T [16] SRAM cells, respectively. The HSNM of the proposed memory cell is 1.21×/1.21×/1.29×/1.21×/1.39×/1.07× times higher than 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16] SRAM cells, respectively. Meanwhile, the RSNM is 1.85×/1.29×/1.3×/1.21×/1.39×/1.08× times higher than 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16] SRAM cells, respectively. This indicates that the proposed cell exhibits better stability during its writing, holding, and reading modes compared to existing cells. For a detailed comparison, please refer the graphical representation is provided in Figure 14. Figures 15–17 present the SNM of all the cells analyzed in this study, along with their butterfly curves illustrating different modes of various bit cells, respectively.

3.1.3 | Delay Analysis

The time interval between the WL voltage reaching 50% and the storage node Q reaching 90% of the BL value is known as the write delay (W_D) or write time (Figure 18a) [25]. As for the 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], 12T [16], and proposed 9T SRAM cells, their respective write delays are 95.1, 101, 97.4, 98.9, 112.5, 117.6, and 95.1 pS. In particular, the write time of the proposed cell is 1.06×, 1.02×, 1.04×, 1.18×, and 1.24× times less than those of the 8T [12], 10T [13], 10T [14], 10T [15], and 12T [16], respectively. The read delay (R_D) of a cell is calculated by delaying the RBL's discharge by 50 mV from the VDD level after the RC is triggered (Figure 18b) [25]. The 6T [8], 8T [12], 10T [13], 10T [14], 10T [15], 12T [16], and proposed 9T SRAM cells R_D is 41.9 , 27.5, 66.5, 33.6, 38.9, 44.5, 50.6, and 39.6 pS, respectively. In particular, the read time of the proposed cell is 1.05×, 1.67×, and 1.12× times less than those of the 6T [8], 10T [13], and 12T [16], respectively. Figure 19 shows a comparison of latency between several SRAM cells.

3.2 | Proposed 9T Cell Performance Across Parameter Variations

The power and noise characteristics of various SRAM cells are examined for CNTFET parameter variation and Process, Voltage, and Temperature (PVT) variation. The essential parameters of CNTFET for simulation are summarized in Table 2. It is observed and reported how the SRAM cells respond to changes in VDD (ranging from 0.6 to 1.2 V), T_{ox} (±20% from its nominal

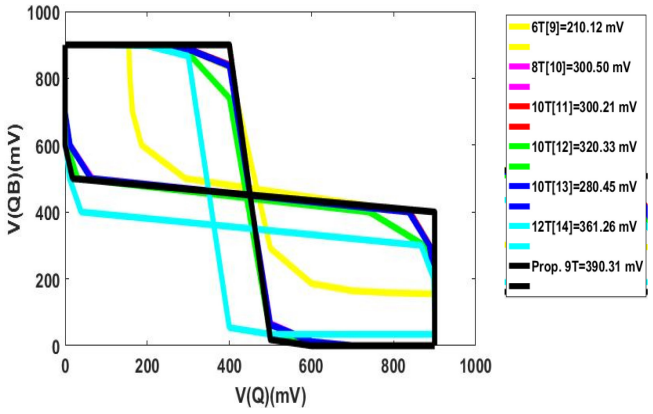

FIGURE 17 | Read SNM butterfly curve of various SRAM cells.

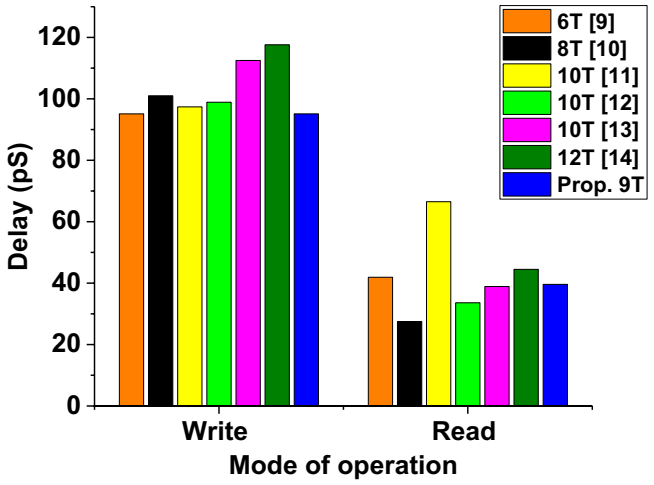

FIGURE 19 | Delay comparison of various SRAM cells.

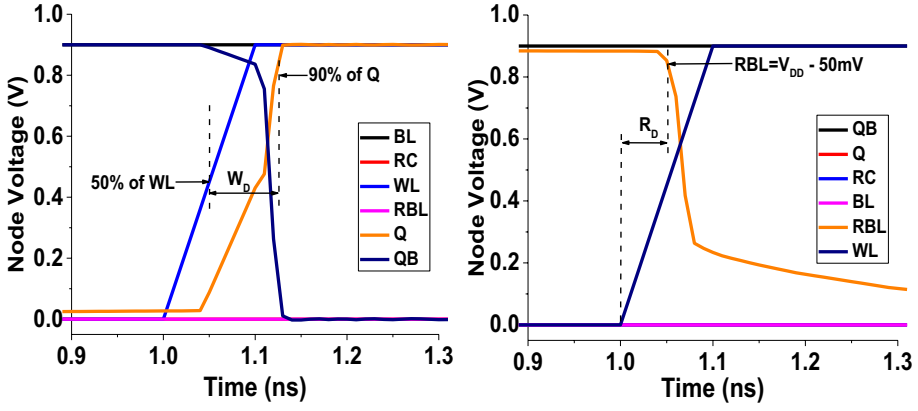

FIGURE 18 | Delay calculation: (a) write "1" operation and (b) read "0" operation.

TABLE 2 | CNTFET parameters for simulation.

Sl. No	Parameters	Nominal value (variation)
1	T_{ox}—Oxide thickness	4 nm (± 20%)
2	*K*—Dielectric constant	HfO_2 = 16 (3.9, 7.5, 10, 16, 25, and 80)
3	*S*—Pitch	20 nm (±20%)
4	VDD—Supply	0.9 V (0.6–1.2)
5	*T*—Temperature	27 (−50, 0, 27, 50, 100, and 150)
6	L_{ch}—Channel length	32 nm
7	*m*, *n*—Chiral vectors	19, 0
8	*N*—Number of CNTs	4

value), *K* (ranging from 3.9 to 80), and *T* (ranging from −50°C to 150°C).

The selection of the gate dielectric constant material for CNTFET significantly influences the performance of a memory cell [11]. The *K* of various materials such as SiO_2 (silicon dioxide), Si_3N_4 (silicon nitride), Al_2O_3 (aluminum oxide), HfO_2 (hafnium oxide), Ta_2O_5 (tantalum pentoxide), and TiO_2 (titanium oxide) are 3.9, 7.5, 10, 16, 25, and 80, respectively. The drain current is proportional to the *K* of the CNTFET. Therefore, an increase in the *K* leads to higher channel current, subsequently elevating the device's power consumption of the memory cell. Furthermore, the Vth of the CNTFET and *K* are inversely related. Hence, an increase in the *K* value reduces the Vth, consequently reducing the stability of the memory cell. The impact of changing the *K* on power consumption and SNM of various SRAM memory cells during different modes is observed. Figures 20 and 21 illustrate the power and SNM variation of SRAM memory cells for different *K* values, respectively.

Temperature fluctuations can swiftly impact memory cells. As the *T* rises, the CNT generates thermally produced electrons

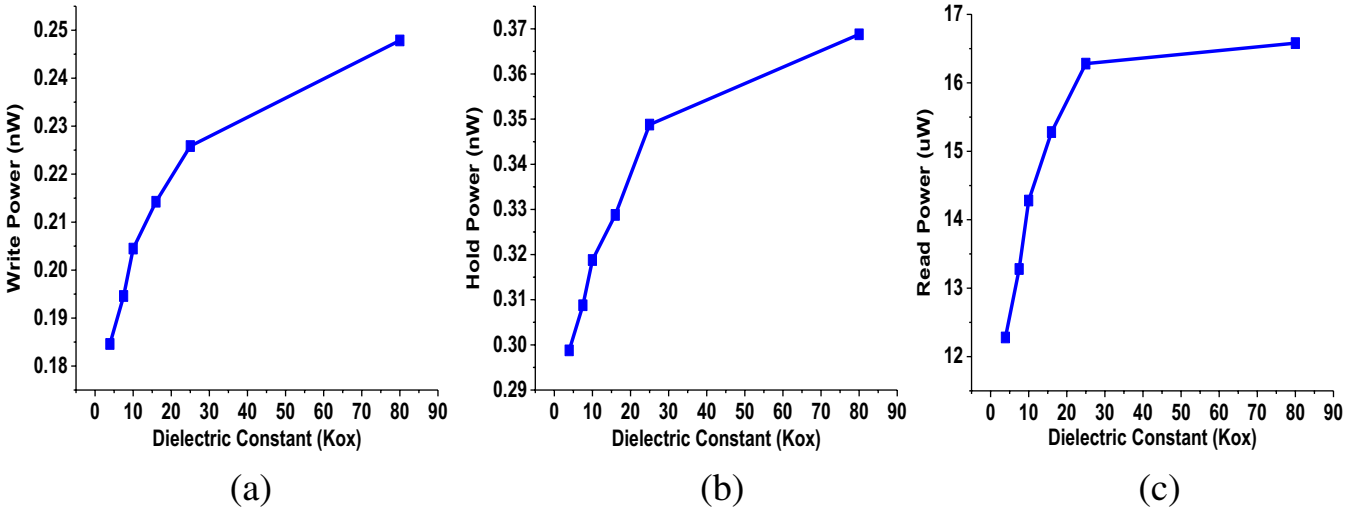

FIGURE 20 | Power versus dielectric constant.

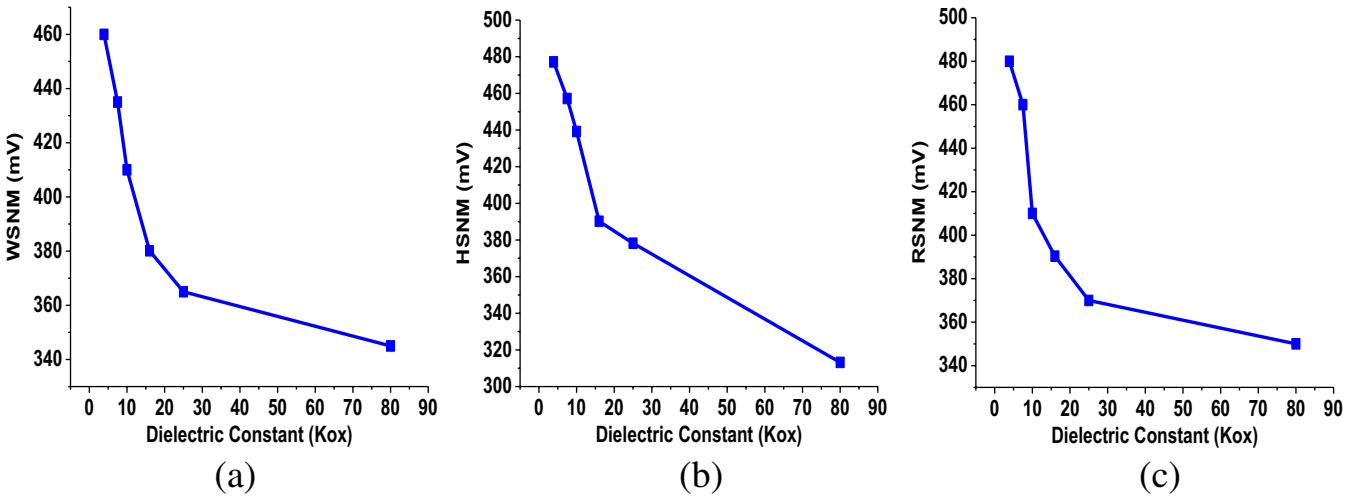

FIGURE 21 | SNM versus dielectric constant.

in the CNTFET, leading to an increase in the channel current. Even at low gate terminal voltages, the presence of thermal charges in the channel is adequate to switch the device "ON." Consequently, as T increases, the Vth of the CNTFET decreases, resulting in a reduction in SNM and an increase in power consumption [26–28]. The performance of various SRAM cells under different operation modes is evaluated across negative temperatures (−50°C), room temperature (27°C), and above room temperature (150°C). This temperature range covers a spectrum of applications ranging from industry, commercial, to military applications. Figures 22 and 23 depict the variation in power consumption and SNM of memory cells for various temperature ranges, respectively.

The SNM and power consumption of SRAM cells are notably affected by the gate oxide thickness of CNTFETs [29–31]. To understand this influence, the power and noise characteristics of SRAM memory cells are evaluated by varying the T_{ox} from 3.2 to 4.8 nm. The T_{ox} directly affects the Vth. Consequently, as the T_{ox} increases, the Vth of the CNTFET also increases. This leads to a reduction in power consumption and an increase in the noise margin of the memory cells. Figures 24 and 25 illustrate the variations in power and SNM values of different SRAM cells in response to changes in T_{ox}, respectively.

The operating voltage of the cell varies within the range of 0.6–1.2 V. Across different operating modes, the resulting power consumption and noise margin levels of SRAM cells are measured. It's observed that the VDD exhibits a direct relationship with both the power dissipation and the SNM of SRAM cells [32, 33]. Thus, increasing the supply voltage enhances the SNM and power of the memory cell. The variations of SNM and power consumption concerning the VDD are illustrated in Figures 26 and 27.

3.3 | VDD_{min} and Figure of Merit (FOM)

An SRAM cell's power performance is greatly influenced by its supply voltage. A bit cell's dynamic power drops by a factor

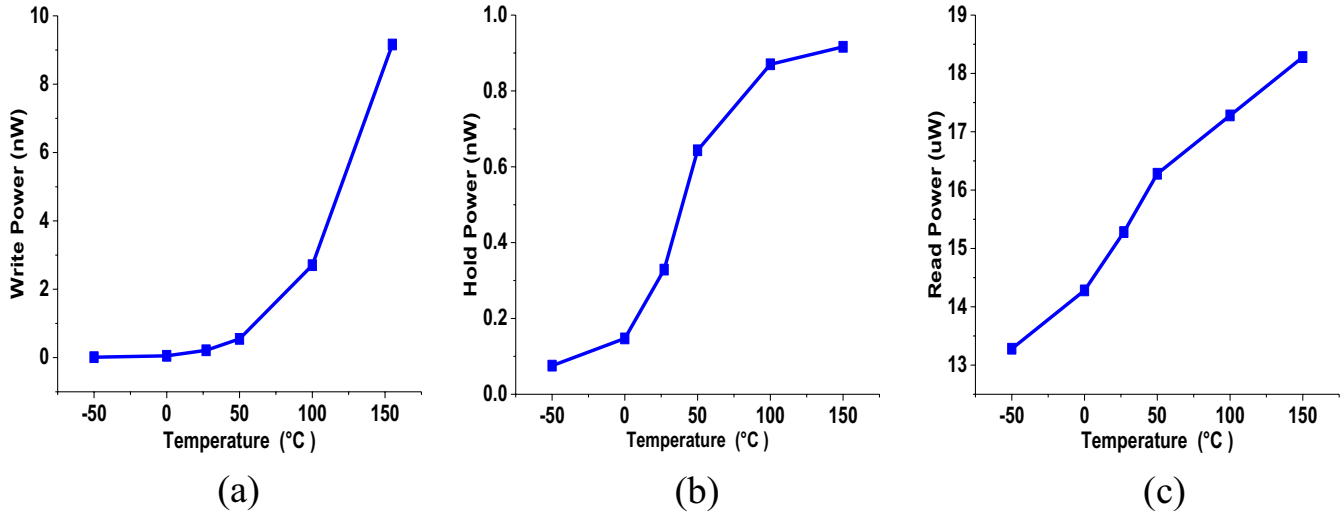

FIGURE 22 | Power versus temperature.

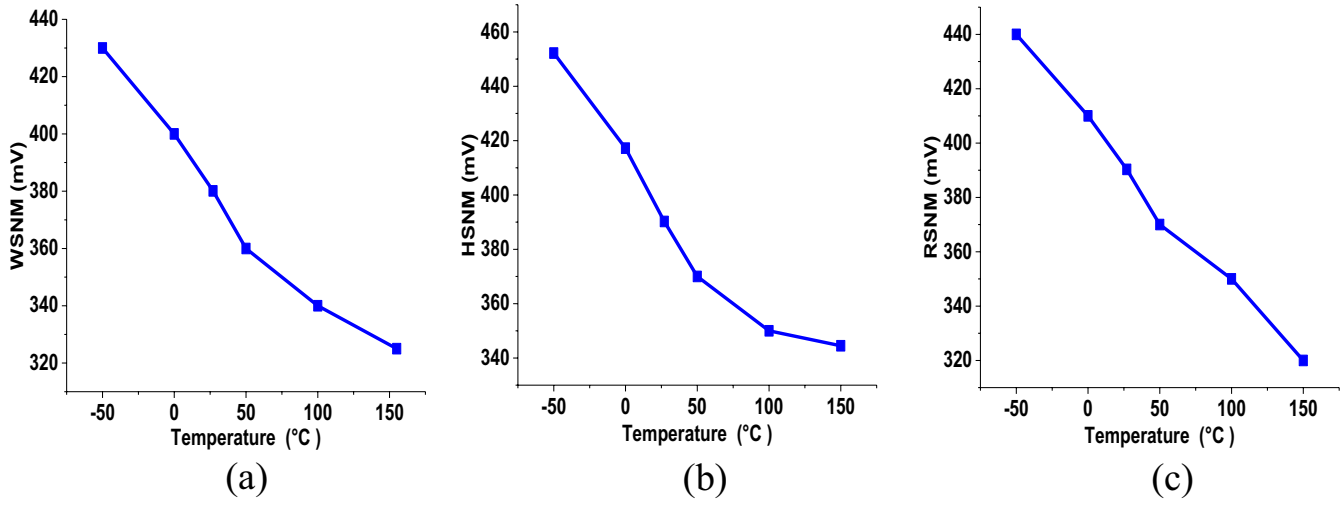

FIGURE 23 | SNM versus temperature.

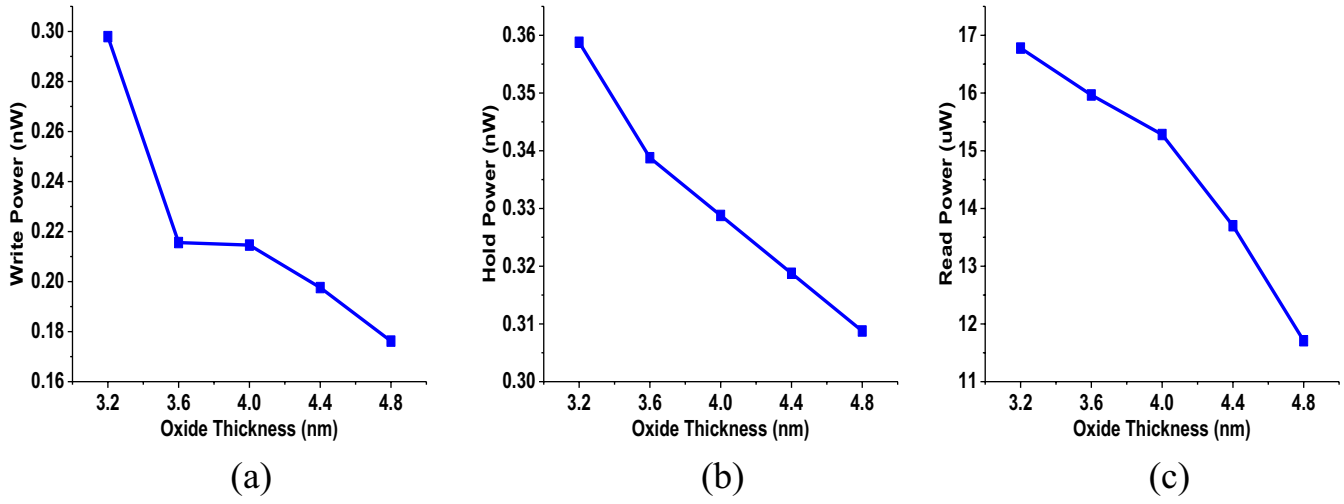

FIGURE 24 | Power versus oxide thickness.

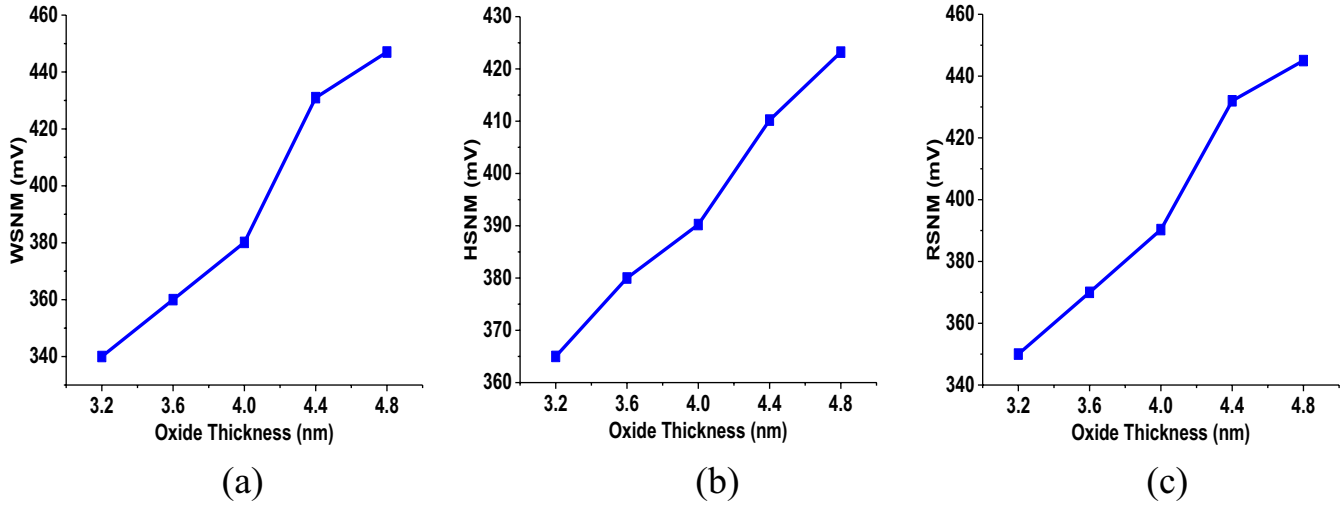

FIGURE 25 | SNM versus oxide thickness.

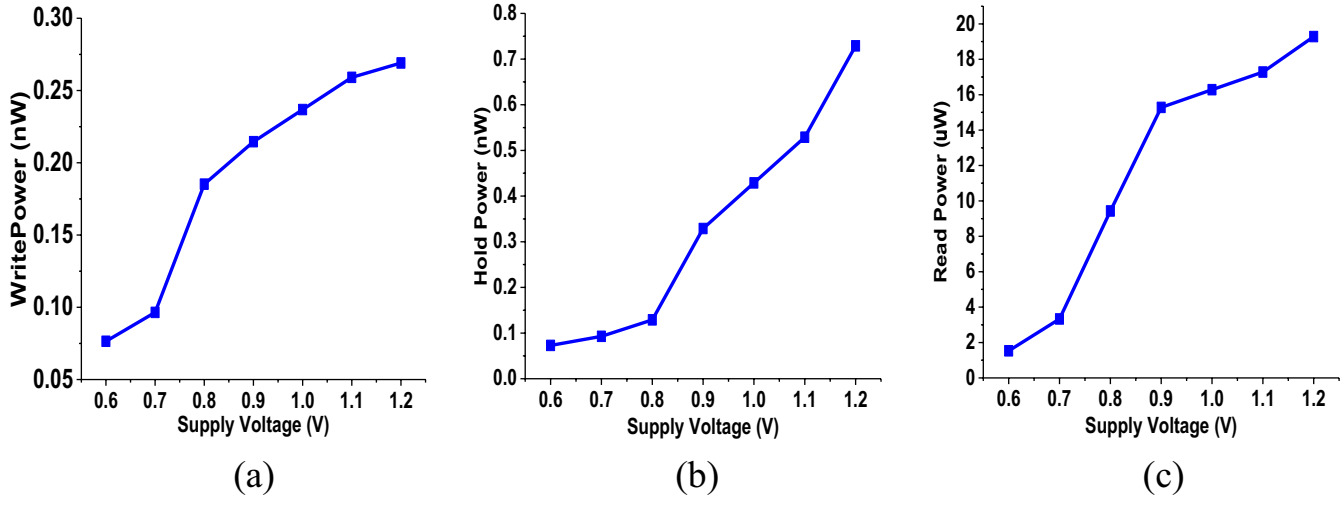

FIGURE 26 | Power versus supply voltage.

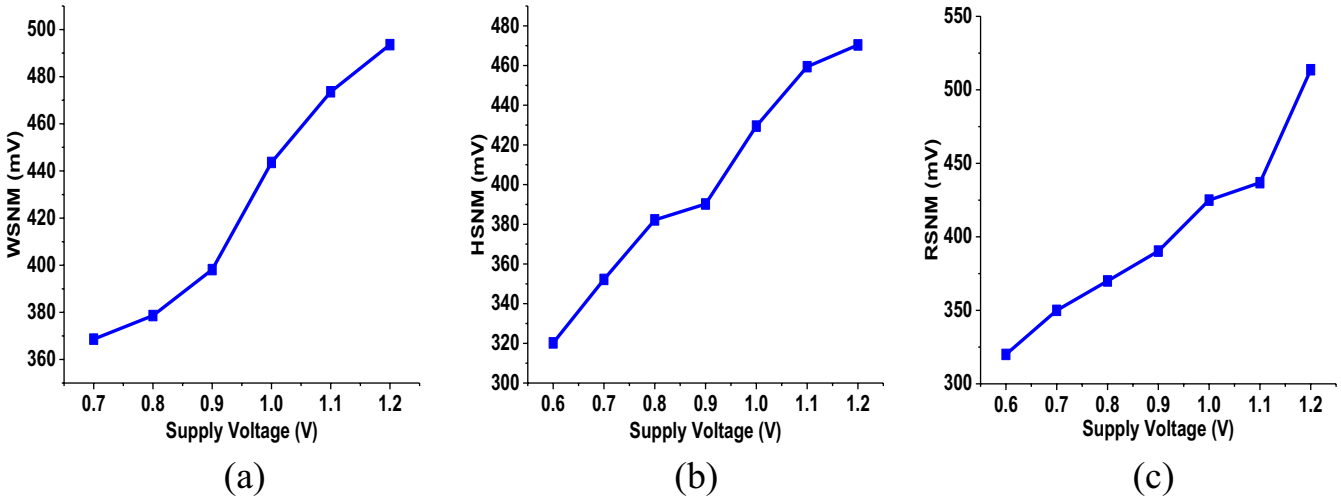

FIGURE 27 | SNM versus supply voltage.

TABLE 3 | Comparison among different CNTFET SRAM cells @V_{DD} = 0.9 V.

SRAM parameters	6T [8]	8T [12]	10T [13]	10T [14]	10T [15]	12T [16]	Prop. 9T
Write power (nW)	0.21	0.21	0.21	0.13	4.32	0.48	0.21
Hold power (μW)	17.47	17.47	17.47	12.22	17.47	13.40	0.00033
Read power (μW)	17.99	18.28	26.00	31.14	22.97	17.59	15.28
Dynamic power (μW)	41.8	41.9	44.41	44.45	43.4	41.6	8.09
WSNM (mV)	240.12	240.12	240.34	310.21	440.35	362.15	380.11
HSNM (mV)	320.02	320.02	300.21	320.46	280.2	364.22	390.22
RSNM (mV)	210.12	300.5	300.21	320.33	280.45	361.26	390.31
Write delay (pS)	95.1	101	97.4	98.9	112.5	117.6	95.1
Read delay (pS)	41.9	27.5	66.5	33.6	38.9	44.5	39.6
Write PDP ($\times 10^{-21}$ J)	20.44	21.71	20.90	13.00	486.29	56.13	20.41
Read PDP ($\times 10^{-18}$ J)	753.6	502.7	1728.7	1046.1	893.3	782.7	605.1
VDD_{min} (mV)	55.8	55.8	67.3	77.5	89.2	78.5	33.6
FOM	1.08×10^{39}	2.17×10^{39}	5.1×10^{38}	2.47×10^{39}	5.11×10^{37}	1.03×10^{39}	4.24×10^{44}

of four and its leakage power drops linearly as the VDD supplied to it is decreased [34, 35, 36]. Therefore, the total power consumption of that bit cell can be decreased by designing an SRAM cell that operates at minimum supply voltage (VDD_{min}). An SRAM cell's VDD_{min} is the operating voltage required to maintain its WSNM at zero and its RSNM and HSNM values at 26 mV (thermal voltage) [25]. The following is the equation-related VDD_{min} [25].

$$VDD_{min} = \text{Max}\{(VDD@HSNM = RSNM = 26\,mV), VDD\,(@WSNM = 0\,V)\} \quad (7)$$

6T [8], 8T [12], 10T [13], 10T [14], 10T [15], 12T [16], and proposed 9T SRAM cells are 55.8, 55.8, 67.3, 77.5, 89.2, 78.5, and 33.6 mV. The VDD_{min} of the proposed bit cell is lower than other cells.

The figure of merit (FOM) of a bit cell is the ratio of the products of WSNM, HSNM, and RSNM to the products of hold power, write power delay product (PDP), read PDP, and VDD_{min}. A good memory cell must have a very large SNM, very low power, and low delay in order to achieve high FOM. The FOM in Equation (8) is provided below. The FOM is computed and reported for every cell utilized in the comparative research. Given that it outperforms other cells in 32 nm CNTFET technology at VDD = 0.9 V, it is evident that the proposed 9T CNTFET bit cell has a very high FOM (Table 3).

$$FOM = \frac{(WSNM \times HSNM \times RSNM)}{(\text{Hold power} \times \text{Write PDP} \times \text{Read PDP} \times VDD_{min})} \quad (8)$$

TABLE 4 | Comparison of proposed SRAM cell's CNTFET and MOSFET implementation.

Parameters	9T MOSFET	9T CNTFET	% of Improvement of a 9T CNTFET-SRAM than MOS-SRAM
Write power (nW)	0.456	0.2145	52.96
Hold power (μW)	0.000741	0.000328	55.73
Read power (μW)	40.81	15.28	62.55
Dynamic power (μW)	21.8	8.09	62.88
WSNM (mV)	374.1	380.11	1.58
HSNM (mV)	351.6	390.22	9.89
RSNM (mV)	351.6	390.31	9.89

3.4 | Comparison of Proposed SRAM Cell's CNTFET and MOSFET Implementation

The proposed SRAM cell also is implemented using 32 nm MOSFET technology, and its performance is compared with that of CNTFET technology (see Table 4). The comparison reveals significant improvements in various parameters of the 9T CNTFET-SRAM over MOS-SRAM. Notably, the 9T CNTFET demonstrates approximately 52.96% lower write power consumption compared to the MOSFET counterpart, showcasing notable energy efficiency. Similarly, the hold power and read power requirements of the CNTFET are reduced by approximately 55.73% and 62.55%, respectively, indicating substantial advancements in power efficiency. Furthermore, the CNTFET exhibits significantly lower dynamic power consumption, with a reduction of approximately 62.88% compared to the MOSFET. While enhancements in WSNM are marginal at 1.58%, notable improvements in HSNM and RSNM, each approximately 9.89%, suggest improved stability and reliability in circuit operations. These findings highlight the promising potential of CNTFET technology in enhancing the performance and efficiency of SRAM designs compared to traditional MOSFETs.

4 | Conclusion

In conclusion, our research presents a pioneering approach in the design of CNTFET-based 9T SRAM cell, incorporating a single-ended read decoupled technique. Through meticulous simulation and analysis using state-of-the-art 32 nm CNTFET models, we unveil remarkable advancements in power efficiency and noise reduction compared to prior works. The demonstrated reductions in power consumption, along with notable enhancements in stability, underscore the significance of our proposed SRAM cell for contemporary memory system design. Furthermore, our findings suggest promising avenues for future research, including the integration of our SRAM cell arrays with sense amplifiers, paving the way for enhanced performance in wireless sensor networks and addressing the evolving demands of modern computing systems. The study's prospects include creating an array of the recommended SRAM cells and combining them with sense amplifiers. The proposed SRAM cell may contribute to meeting VLSI circuits' increasing power, noise, and speed requirements [37–39].

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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